

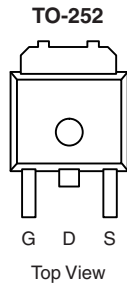


P-Channel 40-V (D-S) 175 °C MOSFET

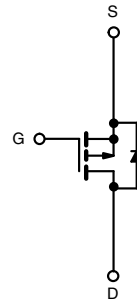
PRODUCT SUMMARY		
V _{DS} (V)	r _{DS(on)} (Ω)	I _D (A)
- 40	0.013 at V _{GS} = - 10 V	- 60 ^a
	0.022 at V _{GS} = - 4.5 V	- 48

FEATURES

- TrenchFET[®] Power MOSFET
- 175 °C Junction Temperature



Drain Connected to Tab



Ordering Information: SUD50P04-13L-E3 (Lead (Pb)-free)

P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS T _A = 25 °C, unless otherwise noted			
Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V _{DS}	- 40	V
Gate-Source Voltage	V _{GS}	± 20	
Continuous Drain Current ^b	I _D	T _C = 25 °C	- 60 ^c
		T _C = 100 °C	- 43
Pulsed Drain Current	I _{DM}	- 100	
Continuous Source Current (Diode Conduction)	I _S	- 60 ^c	
Avalanche Current	I _{AS}	L = 0.1 mH	- 40
Avalanche Energy,			E _{AS}
Maximum Power Dissipation ^b	P _D	T _C = 25 °C	93.7 ^b
		T _A = 25 °C	3 ^a
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 175	°C

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient ^a	R _{thJA}	t ≤ 10 sec	15	18	°C/W
		Steady State	40	50	
Maximum Junction-to-Case (Drain)	R _{thJC}	1.3	1.8		

Notes:

a. Surface Mounted on 1" x 1" FR4 board.

b. See SOA curve for voltage derating.

b. Calculated based on maximum allowed Junction Temperature. Package limitation current is 50 A.

SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	-40			V
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	-1.0		-3.0	
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -40\text{ V}, V_{GS} = 0\text{ V}$			-1	μA
		$V_{DS} = -40\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$			-50	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} = -5\text{ V}, V_{GS} = -10\text{ V}$	-50			A
Drain-Source On-State Resistance ^a	$r_{DS(on)}$	$V_{GS} = -10\text{ V}, I_D = -30\text{ A}$		0.0105	0.013	Ω
		$V_{GS} = -10\text{ V}, I_D = -30\text{ A}, T_J = 125\text{ }^\circ\text{C}$			0.020	
		$V_{GS} = -4.5\text{ V}, I_D = -20\text{ A}$		0.017	0.022	
Forward Transconductance ^a	g_{fs}	$V_{DS} = -15\text{ V}, I_D = -30\text{ A}$	15			S
Dynamic^b						
Input Capacitance	C_{iss}	$V_{DS} = -25\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		3120		pF
Output Capacitance	C_{oss}			440		
Reverse Transfer Capacitance	C_{rss}			320		
Gate Resistance	R_g	$f = 1\text{ MHz}$		4.3		Ω
Total Gate Charge ^c	Q_g	$V_{DS} = -20\text{ V}, V_{GS} = -10\text{ V}, I_D = -50\text{ A}$		63	95	nC
Gate-Source Charge ^c	Q_{gs}			13		
Gate-Drain Charge ^c	Q_{gd}			16		
Turn-On Delay Time ^c	$t_{d(on)}$	$V_{DD} = -20\text{ V}, R_L = 0.4\text{ }\Omega$ $I_D \cong -50\text{ A}, V_{GEN} = -10\text{ V}, R_g = 2.5\text{ }\Omega$		15	25	ns
Rise Time ^c	t_r			18	30	
Turn-Off Delay Time ^c	$t_{d(off)}$			60	90	
Fall Time ^c	t_f			47	70	
Drain-Source Body Diode Characteristics						
Pulse Current	I_{SM}				-100	
Forward Voltage ^a	V_{SD}	$I_F = -50\text{ A}, V_{GS} = 0\text{ V}$		-1.0	-1.5	V
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = -50\text{ A}, di/dT = 100\text{ A}/\mu\text{s}$		36	55	ns

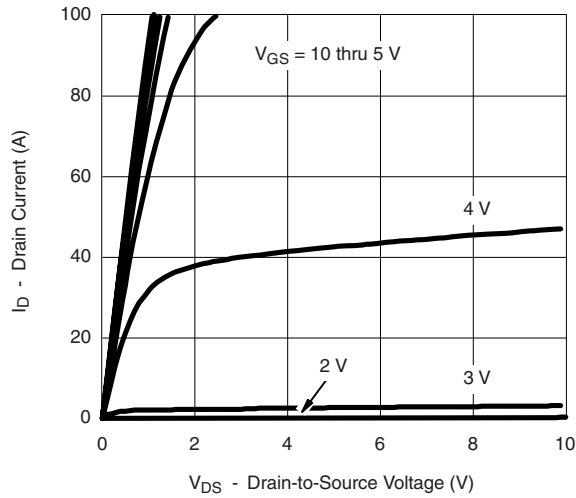
Notes:

- Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
- Guaranteed by design, not subject to production testing.
- Independent of operating temperature.

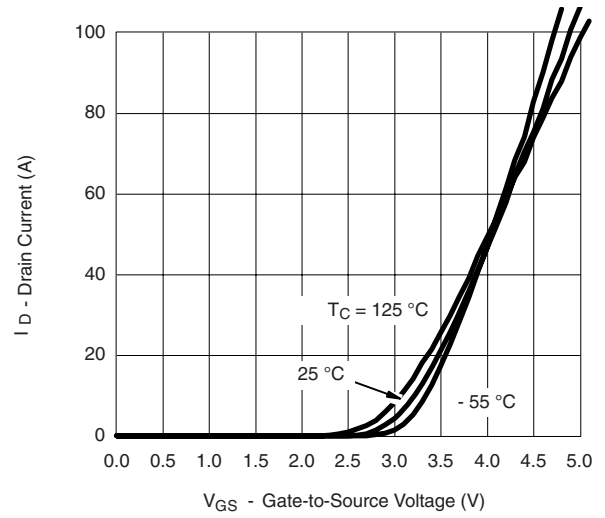
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



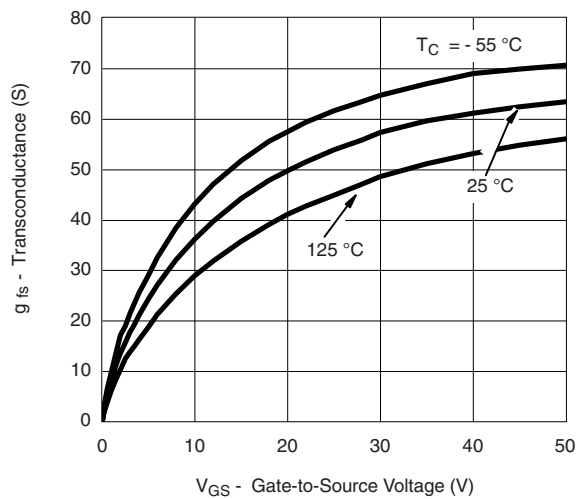
TYPICAL CHARACTERISTICS 25 °C unless noted



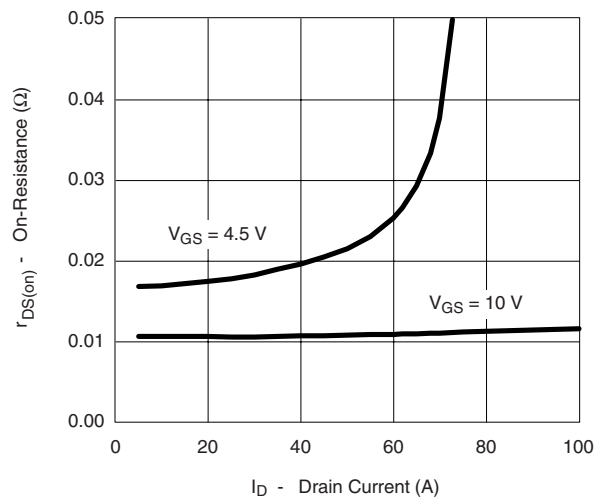
Output Characteristics



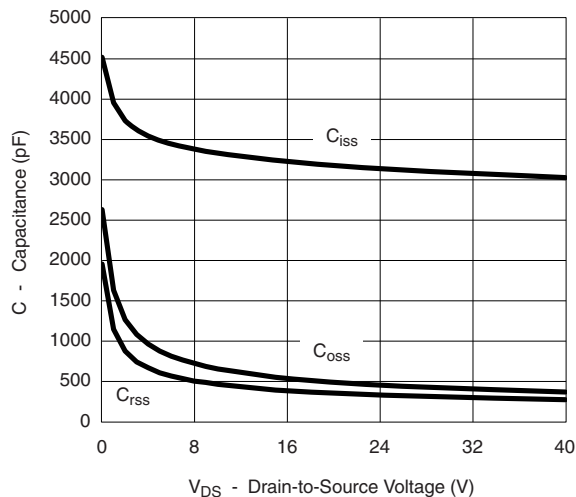
Transfer Characteristics



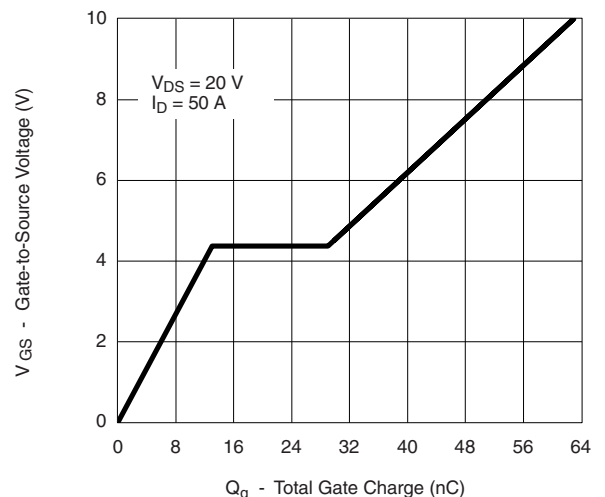
Transconductance



On-Resistance vs. Drain Current



Capacitance



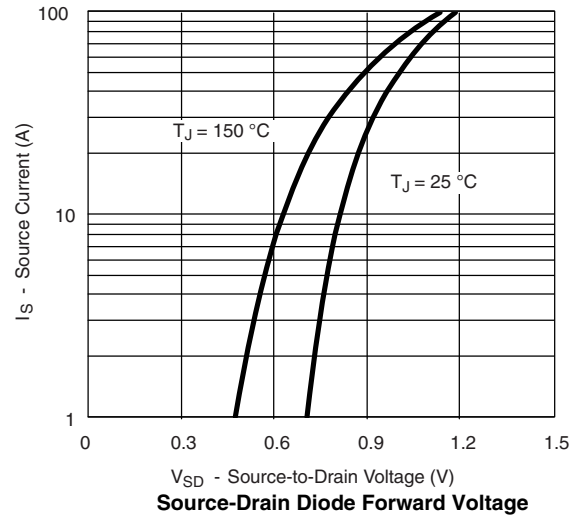
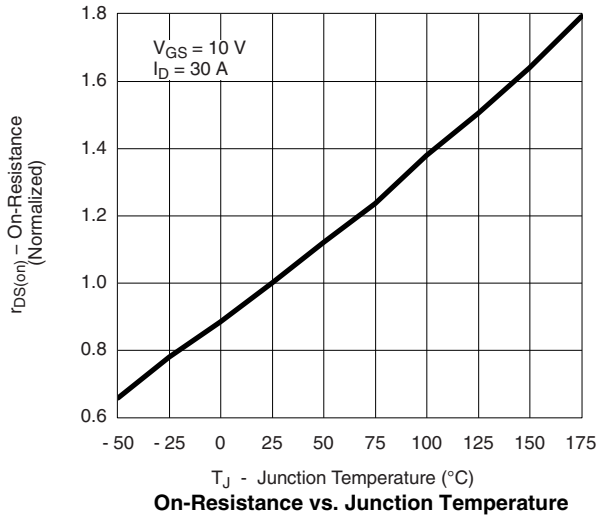
Gate Charge

SUD50P04-13L

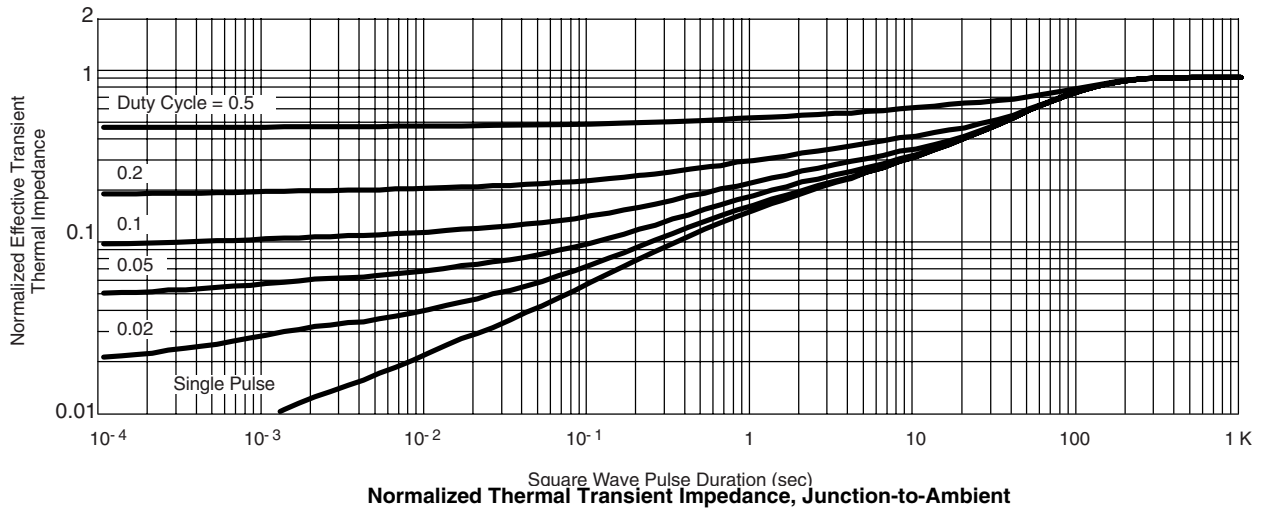
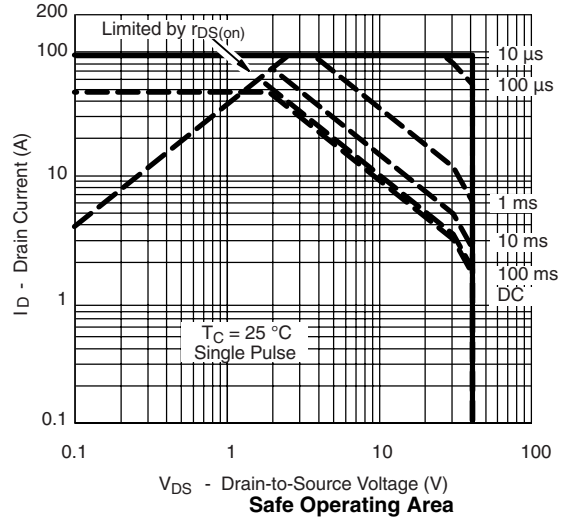
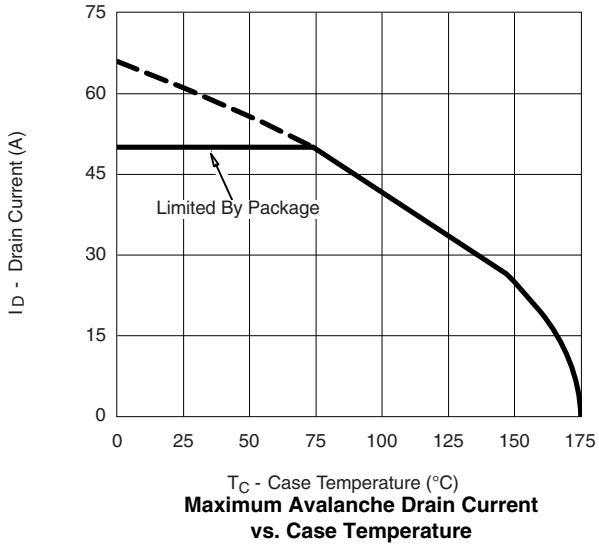


Vishay Siliconix

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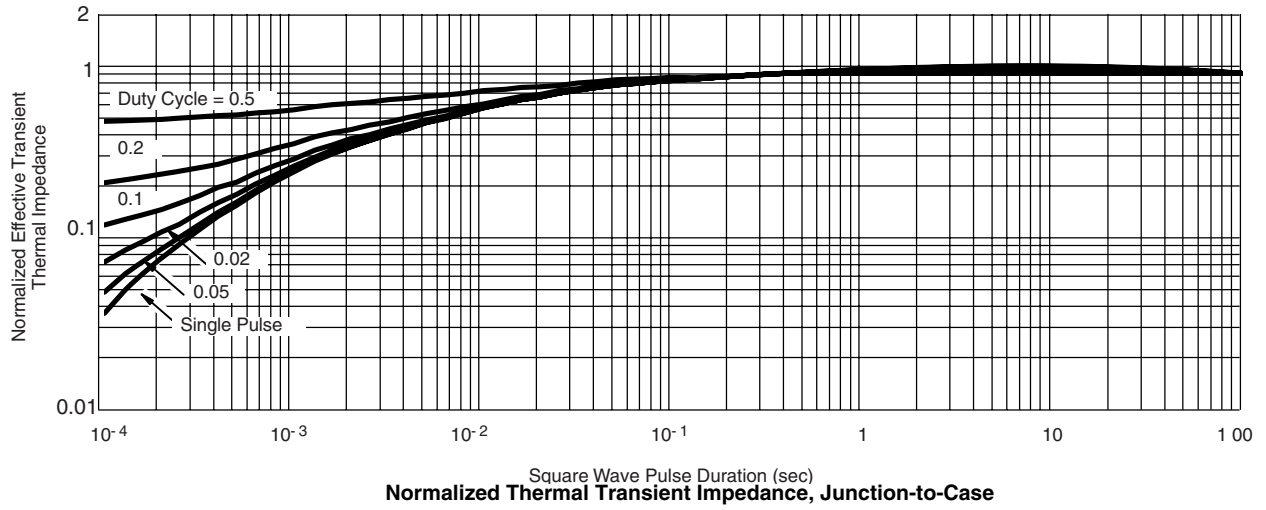


THERMAL RATINGS





THERMAL RATINGS



Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <http://www.vishay.com/ppg?73009>



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