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Evaluation Board for the ADP5054 4-Channel Power Management Unit

FEATURES

- **Wide input voltage range: 4.5 V to 15.5 V**
- **Full featured evaluation board for the ADP5054**
  - **Channel 1: programmable 2 A/4 A/6 A buck regulator**
  - **Channel 2: programmable 2 A/4 A/6 A buck regulator**
  - **Channel 3: 2.5 A sync buck regulator**
  - **Channel 4: 2.5 A sync buck regulator**
- **Standalone operation capability**
- **Cascading options for four buck regulators**
- **Dedicated enable option for each channel**
- **Mode option to select power savings mode (PSM) or forced pulse width modulation (FPWM) operation**
- **Programmable switching frequency from 250 kHz to 2 MHz**
- **Frequency synchronization input or output**

EQUIPMENT NEEDED

- **Input power source**
- **Voltmeter**
- **Ammeter**
- **Load resistors or electrical load**

GENERAL DESCRIPTION

This user guide describes the evaluation of the ADP5054 and includes detailed schematics and printed circuit board (PCB) layouts.

The ADP5054 evaluation board combines four high performance buck regulators in a 48-lead LFCSP package to meet the demanding performance and board space requirements. The ADP5054 evaluation board connects to high input voltages, up to 15 V directly without any preregulators.

Full details on the device are provided in the ADP5054 data sheet, and it is recommended that the data sheet be consulted in conjunction with this evaluation board user guide.

ADP5054 EVALUATION BOARD

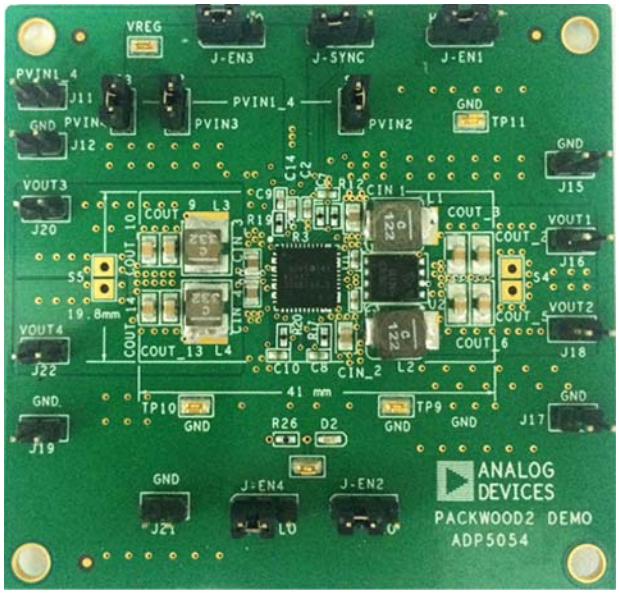

Figure 1.

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REVISION HISTORY

3/15—Revision 0: Initial Version

USING THE EVALUATION BOARD

POWERING UP THE EVALUATION BOARD

The ADP5054 evaluation board is supplied fully assembled and tested. Before applying power to the evaluation board, follow the procedures in this section.

Enable Jumpers

Each channel has its own enable pin that must be pulled high to enable that channel (see Table 1). Pull the enable pin low or leave it floating to disable the channel.

The enable control for each regulator has a 0.811 V precision enable threshold that allows the ADP5054 to be easily sequenced between channels or other input/output supplies. The enable control can also be used as a programmable undervoltage lockout (UVLO) input by the resistor divider.

Table 1. Channels of the Enable Pins

Channel	Pin	Enable Jumper	Description
Channel 1: Buck	EN1	J-EN1	0.8 V precision enable
Channel 2: Buck	EN2	J-EN2	0.8 V precision enable
Channel 3: Buck	EN3	J-EN3	0.8 V precision enable
Channel 4: Buck	EN4	J-EN4	0.8 V precision enable

Power Input Jumpers

Each channel except Channel 1 has its own power input jumper, which allows the device to support separate input voltage or cascaded options for all channels. Channel 1 input voltage is tied to PVIN1_4 and does not need a jumper.

The power input for the buck regulators is 4.5 V to 15.5 V. Shunt S1, S2, and S3 to allow the easy setup of Channel 2, Channel 3, and Channel 4 using the same input voltage with Channel 1 for the buck regulators.

Table 2. Channels of Power Input Jumpers

Channel	Pin	Input Jumper	Input Range
Channel 2: Buck	PVIN2	S1	4.5 V to 15.5 V
Channel 3: Buck	PVIN3	S2	4.5 V to 15.5 V
Channel 4: Buck	PVIN4	S3	4.5 V to 15.5 V

Jumper J-SYNC (SYNC/MODE)

The J-SYNC jumper (shown in Figure 1) connects the SYNC/MODE pin of the device to either low or high.

Shunt the center contact of the J-SYNC jumper (SYNC/MODE) to the left pin header so that the SYNC/MODE pin is pulled high to VREG (5 V). This connection switches the buck regulators into FPWM operation.

Shunt the center contact of the J-SYNC jumper to the right pin header to pull the SYNC/MODE pin low, which forces the buck regulators to operate in automatic PWM/PSM operation.

Input Power Source

Before connecting the power source to the ADP5054 evaluation board, turn the evaluation board off. If the input power source includes a current meter, use that meter to monitor the input current. Connect the positive terminal of the power source to the PVIN1_4 terminal (J11) on the evaluation board, and the negative terminal of the power source to the GND terminal (J12) of the board. If the power source does not include a current meter, connect a current meter in series with the input source voltage. Connect the positive terminal of the power source to the positive (+) lead of the current meter, the negative terminal of the power source to the GND terminal (J12), and the negative (−) lead of the current meter to the PVIN1_4 terminal (J11).

Output Load

Turn the board off before connecting the load. Connect an electronic load or resistor to set the load current. If the load includes an ammeter, or if the current is not measured, connect the load directly to the evaluation board, with the positive (+) load connected to one of the channels. For example, connect Buck 1, VOUT1 (J16), and the negative (−) load connection to GND (J15).

If an ammeter is used, connect it in series with the load. Connect the positive (+) ammeter terminal to the evaluation board for Buck 1, VOUT1 (J16), the negative (−) ammeter terminal to the positive (+) load terminal, and the negative (−) load terminal to the evaluation board at GND (J15).

Input and Output Voltmeters

Measure the input and output voltages with voltmeters. Ensure that the voltmeters are connected to the appropriate evaluation board terminals and not to the load or power sources.

If the voltmeters are not connected directly to the evaluation board, the measured voltages are incorrect due to the voltage drop across the leads and/or connections between the evaluation board, the power source, and/or the load.

Connect the input voltage measuring voltmeter positive (+) terminal to the evaluation board at PVIN1_4 (J11). Connect the input voltage measuring voltmeter negative (−) terminal to the evaluation board at GND (J12).

To measure the output voltage of Buck 1, connect the output voltage measuring voltmeter positive (+) terminal to the evaluation board at VOUT1 (J16). Connect the output voltage measuring voltmeter negative (−) terminal to the evaluation board at GND (J15).

Quick Start

Ensure that the power source voltage for the buck regulators (PVIN1, PVIN2, PVIN3, PVIN4) is 4.5 V to 15.5 V. Shunt the S1, S2, and S3 jumpers to use the same input voltage for the buck regulators. Use the J-EN1, J-EN2, J-EN3, J-EN4 jumpers to enable or disable the desired channel.

Figure 2 shows the ADP5054 board connection diagram. When the power source and load are connected to the evaluation board, the board can be powered for operation. If the load is not enabled, enable the load. Verify that the evaluation board is drawing the proper current and that the output voltage maintains voltage regulation.

After power-up, measure the following output voltages:

- V_{OUT1} = 1.2 V, supply up to a 6 A output load
- V_{OUT2} = 1.8 V, supply up to a 6 A output load
- V_{OUT3} = 1.5 V, supply up to a 2.5 A output load
- V_{OUT4} = 3.3 V, supply up to a 2.5 A output load

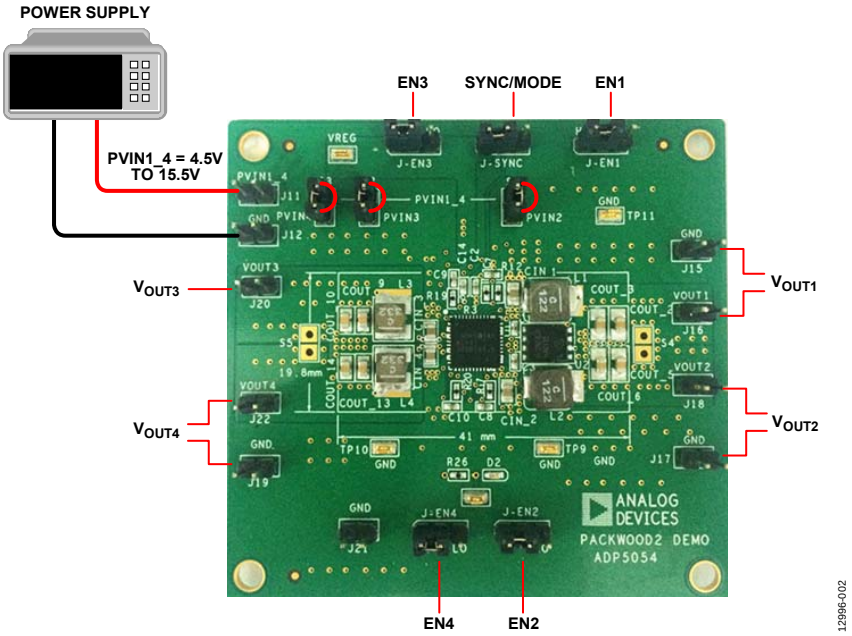

Figure 2. ADP5054 Board Connection Diagram

MEASURING EVALUATION BOARD PERFORMANCE

MEASURING BUCK REGULATOR OUTPUT VOLTAGE RIPPLE

To observe the output voltage ripple of Buck 1, place an oscilloscope probe across the output capacitor (COUT_x) with the probe ground lead at the negative (−) capacitor terminal and the probe tip at the positive (+) capacitor terminal. Figure 3 shows the typical output ripple waveform.

Set the oscilloscope to ac, 10 mV/division, and 2 µs/division time base, with the bandwidth (BW) set to 20 MHz to avoid noise interfering with the measurements. To minimize coupling, shorten the ground loop of the oscilloscope probe. A good way of measuring the output voltage ripple is to solder a wire to the negative (−) capacitor terminal and wrap it around the barrel of the probe, while the tip directly connects to the positive (+) capacitor terminal as shown in Figure 4.

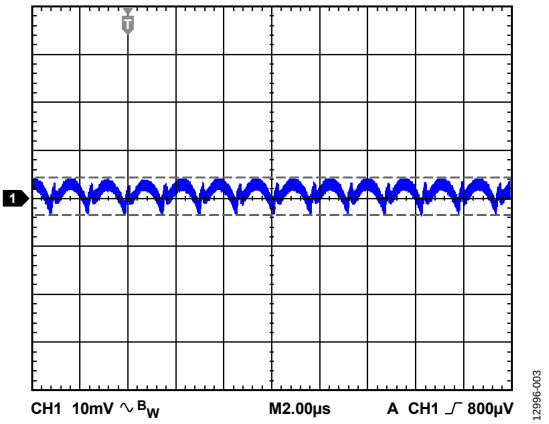

Figure 3. Output Ripple, V_{IN} = 12 V, V_{OUT} = 1.2 V, L = 1 µH, C_{OUT} = 47 µF × 2, f_{SW} = 600 kHz, FPWM Mode

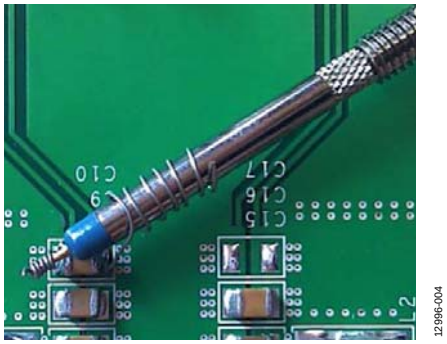

Figure 4. Measuring the Output Voltage Ripple

MEASURING BUCK SWITCHING WAVEFORM

To observe the switching waveform with an oscilloscope, place the oscilloscope probe tip at the end of the inductor with the probe ground at GND. Set the oscilloscope to dc, 5 V/division, and 1 µs/division time base.

When the SYNC/MODE pin is set to high, the buck regulators operate in FPWM mode. When the SYNC/MODE pin is set to low, the buck regulators operate in PSM, which improves the light load efficiency.

Typical PSM and FPWM switching waveforms are shown in Figure 5 and Figure 6.

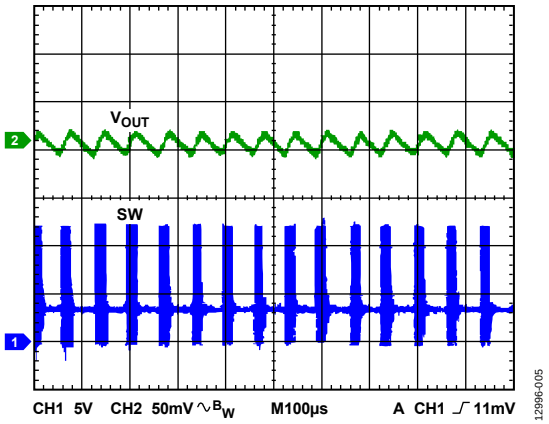

Figure 5. Typical PSM Waveform, V_{IN} = 12 V, V_{OUT} = 3.3 V, I_{OUT} = 3 A, f_{SW} = 600 kHz, L = 4.7 µH, C_{OUT} = 47 µF × 2

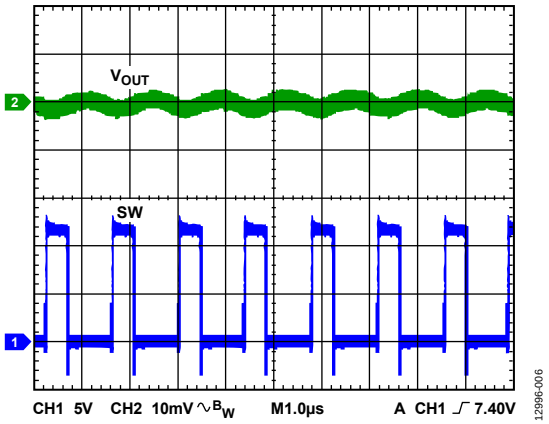

Figure 6. Typical FPWM Mode Waveform, V_{IN} = 12 V, V_{OUT} = 3.3 V, I_{OUT} = 3 A, f_{SW} = 600 kHz, L = 4.7 µH, C_{OUT} = 47 µF × 2

MEASURING SYNCHRONIZATION INPUT OR OUTPUT

The SYNC/MODE pin can be configured as the clock output by setting the CFG34 pin. A clock is generated at the SYNC/MODE pin with the frequency equal to the internal frequency set by the RT pin.

When the SYNC/MODE pin is configured as the input, the ADP5054 can be synchronized to an external clock applied to the SYNC/MODE pin. The internal clock set by the RT pin must be programmed close to the external clock.

MEASURING BUCK LOAD REGULATION

Test the buck load regulation by increasing the load at the output and examining the change in output voltage. The input voltage must be held constant during this measurement. To minimize voltage drop, use short, low resistance wires, especially for loads approaching maximum current. Typical buck load regulation is shown in Figure 7.

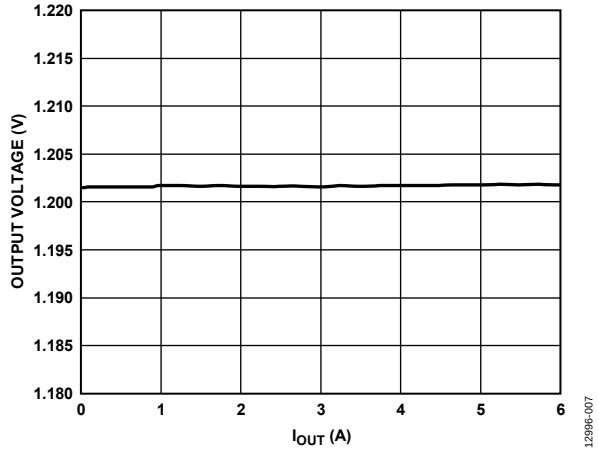

Figure 7. Buck Load Regulation

MEASURING BUCK LINE REGULATION

To measure the buck line regulation, vary the input voltage and examine the change in the output voltage. Typical buck line regulation is shown in Figure 8.

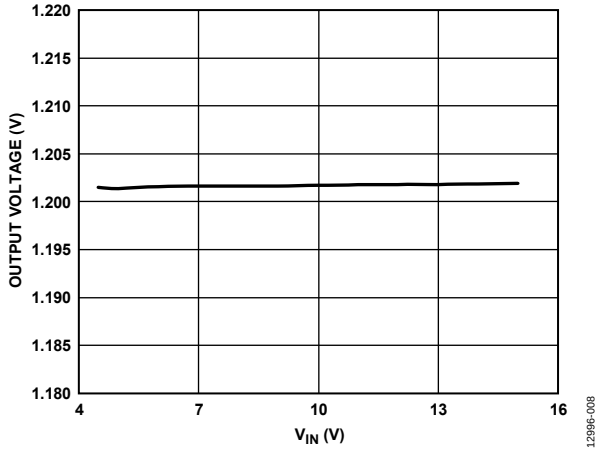

Figure 8. Buck Line Regulation

MEASURING BUCK EFFICIENCY

Measure the efficiency, η, by comparing the input power with the output power.

$$\eta = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times I_{IN}}$$

Measure the input and output voltages as close as possible to the input and output capacitors to reduce the effect of IR drops.

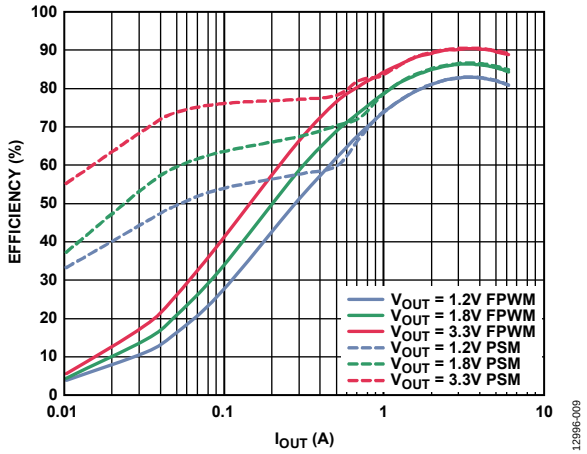

Figure 9. Buck 1/Buck 2 Efficiency, V_{IN} = 12 V, f_{SW} = 600 kHz, MOSFET = SI7232DN, PSM and FPWM Mode

MEASURING INDUCTOR CURRENT

Measure the inductor current by removing one end of the inductor from its pad and connecting a current loop in series. A current probe can be connected to this wire.

MODIFYING THE BOARD

SETTING THE BUCK OUTPUT VOLTAGE (CHANNEL 1 TO CHANNEL 4)

The buck output voltage is set through external resistor dividers, shown in Figure 10 for Buck 1. The output voltage can be factory programmed to default values, as indicated in the ADP5054 data sheet. Connect FB1 to the top of the capacitor on VOUT1 by placing a 0 Ω resistor on R_{TOP}.

In the output adjustable version, the equation for the output voltage setting is

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_{TOP}}{R_{BOT}}\right)$$

where:
V_{OUT} is the output voltage.
V_{REF} is the 0.8 V feedback reference voltage.
R_{TOP} is the feedback resistor from V_{OUT} to FB.
R_{BOT} is the feedback resistor from FB to ground.

The V_{REF} voltage (FB1, FB2, FB3, FB4) for the buck regulators is 0.800 V in the adjustable version.

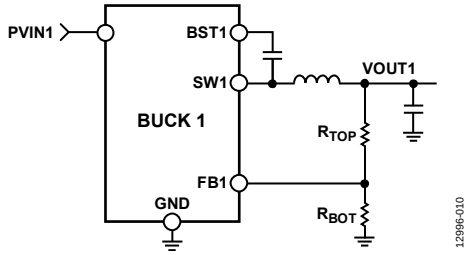

Figure 10. Buck 1 External Output Voltage Setting

When the output voltage of the bucks is changed, the values of inductors, the output capacitors, and the compensation networks must be recalculated and changed for stable operation. See the ADP5054 data sheet for more details on external components selection.

BUCK EXTERNAL RESISTOR DIVIDER SETTING

The ADP5054 evaluation board is supplied with the resistor divider for a target output voltage. Varying the resistor values of the resistor divider networks varies the output voltage accordingly. Table 3 shows the external resistor dividers for each channel.

Table 3. External Resistor Dividers in Each Channel

Resistor Divider	Buck 1	Buck 2	Buck 3	Buck 4
R_{TOP}	R2	R4	R6	R5
R_{BOT}	R28	R29	R31	R30

CHANGING THE SWITCHING FREQUENCY

The switching frequency of the ADP5054 evaluation board is programmed to be 600 kHz. To change the switching frequency, replace the R3 resistor at the RT pin with a different value, as shown in Figure 11.

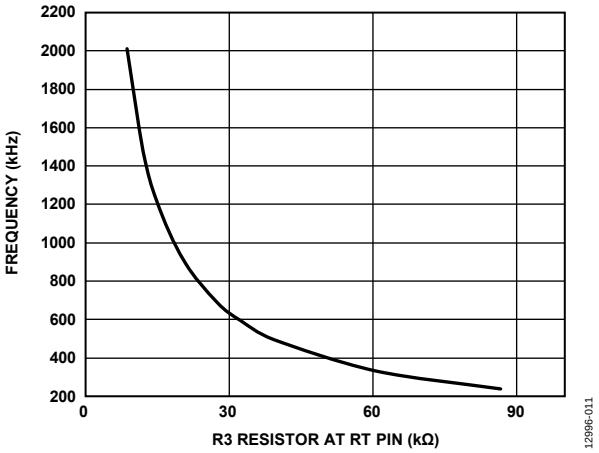

Figure 11. Switching Frequency vs. R3 Resistor at RT Pin

Program the external resistors on the CFG12 and CFG34 pins to set the channel switching frequency to half.

When the switching frequency is changed, the values of the inductors, the output capacitors, and the compensation networks must be recalculated and changed for stable operation. See the ADP5054 data sheet for more details on external components selection.

CHANGING THE PEAK CURRENT-LIMIT THRESHOLD IN CHANNEL 1/CHANNEL 2

The peak current limit of the ADP5054 evaluation board in Channel 1 and Channel 2 is set to 10.4 A.

To change the peak current-limit threshold, replace the R8 resistor for Channel 1 (R7 for Channel 2) with a different value, as shown in Table 4. The programmable current-limit threshold feature allows the use of a small sized inductor for low current applications.

Table 4. Load Capability Settings on Channel 1 and Channel 2

R_{ILIM1}/R_{ILIM2}	I_{OUT} in Channel 1/Channel 2
Floating	4 A, with 6.9 A typical peak current limit
47 kΩ	2 A, with 3.8 A typical peak current limit
22 kΩ	6 A, with 10.4 A typical peak current limit

CHANGING THE SOFT START TIME

The soft start time of the ADP5054 on the evaluation board is programmed to be 2 ms for the buck regulators. To program a different soft start time, replace Resistors R16 and R39 for Channel 1 and Channel 2, respectively, and/or Resistors R40 and R18 for Channel 3 and Channel 4, respectively. See the ADP5054 data sheet for more details.

CONFIGURING CHANNEL 1/CHANNEL 2 AND CHANNEL 3/CHANNEL 4 AS 2-PHASE PARALLEL OUTPUTS

Channel 1 and Channel 2 are programmed as individual outputs in the ADP5054 evaluation board. Channel 3 and Chanel 4 can be configured as individual outputs as well.

To configure Channel 1/Channel 2 as a 2-phase parallel output, the following steps are required:

1. Short the S4 jumper.
2. Change R39 = 400 kΩ and R16 = 300 kΩ (or R39 = 500 kΩ and R16 = 200 kΩ, or R39 = 600 kΩ and R16 = 100 kΩ) in the CFG12 pin setting.
3. Remove R17 and C8 from the COMP2 pin.
4. Remove R4, and replace R29 with 0 Ω on the FB2 pin.
5. Shunt the J-EN2 jumper to low.
6. Use the FB1 pin (R2 and R28) to set the output voltage.
7. Use the J-EN1 jumper (EN1 pin) to enable or disable the regulator.

To configure Channel 3/Channel 4 as a 2-phase parallel output, the following steps are required:

1. Short the S5 jumper.
2. Change R40 = 300 kΩ and R18 = 400 kΩ (or R40 = 400 kΩ and R18 = 300 kΩ, or R40 = 500 kΩ and R18 = 200 kΩ) in the CFG34 pin setting.
3. Remove R20 and C10 from the COMP4 pin.
4. Remove R5, and replace R30 with 0 Ω on the FB4 pin.
5. Shunt the J-EN4 jumper to low.
6. Use the FB3 pin (R6 and R31) to set the output voltage.
7. Use the J-EN3 jumper (EN3 pin) to enable or disable the regulator.

During the parallel configuration, the input voltage and the current-limit threshold for both channels are the same, and FPWM operation on Channel 1, Channel 2, Channel 3, and Channel 4 is recommended. See the ADP5054 data sheet for more details on configuring as a 2-phase parallel output.

EVALUATION BOARD SCHEMATIC AND ARTWORK

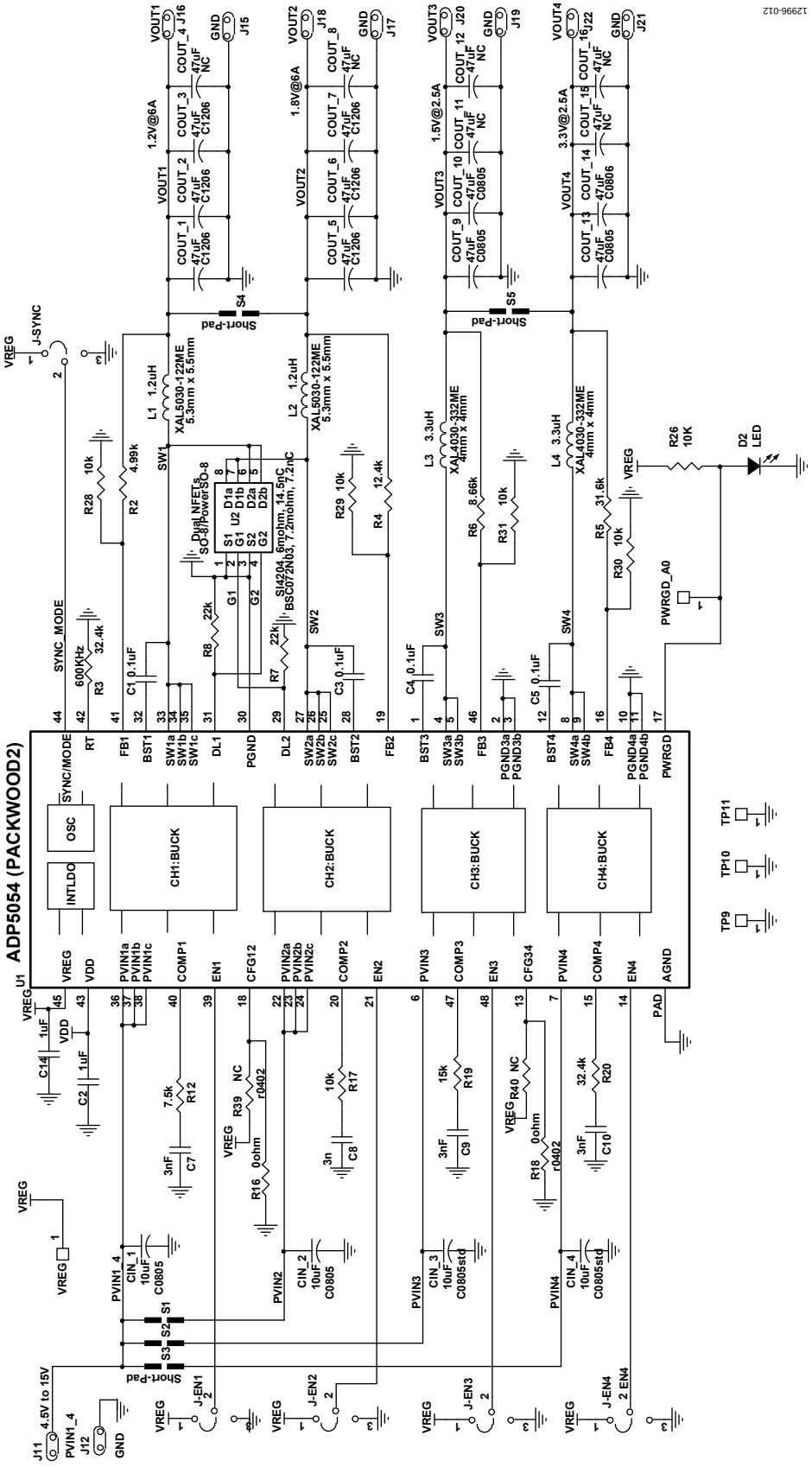

Figure 12. ADP5054 Evaluation Board Schematic

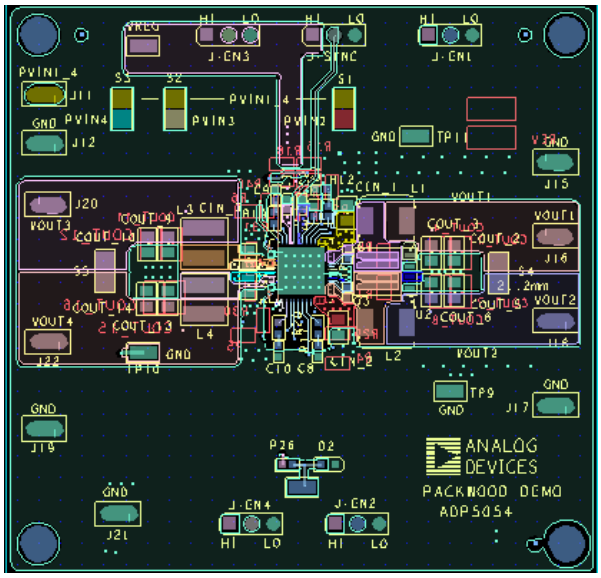

Figure 13. ADP5054 Evaluation Board Recommended Layout, Top Layer

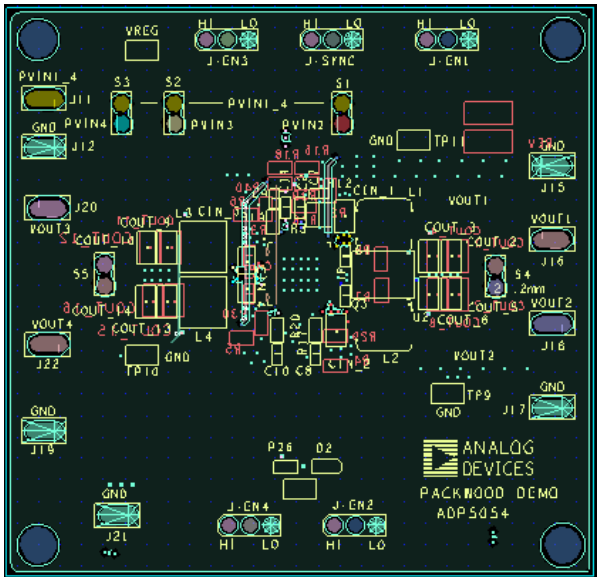

Figure 14. ADP5054 Evaluation Board Recommended Layout, Layer 2

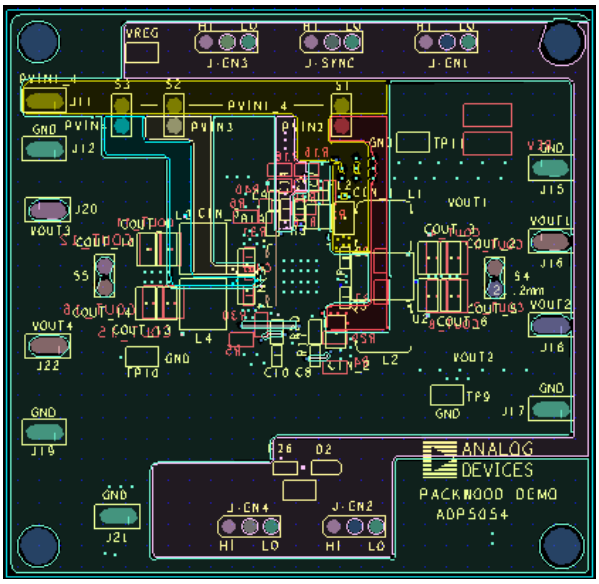

Figure 15. ADP5054 Evaluation Board Recommended Layout, Layer 3

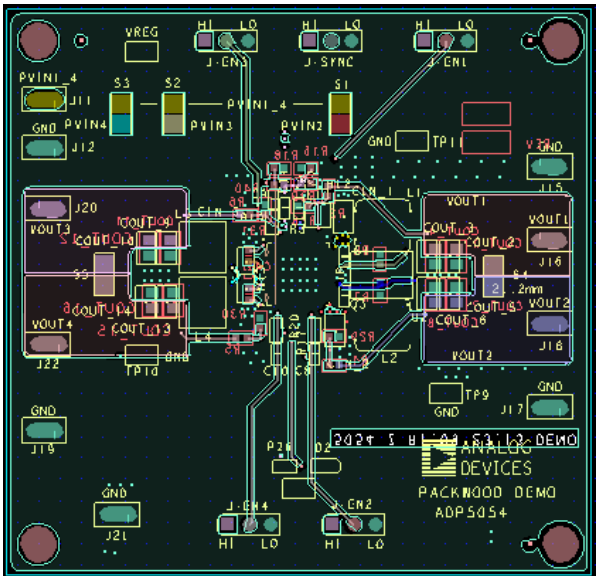

Figure 16. ADP5054 Evaluation Board Recommended Layout, Bottom Layer

ORDERING INFORMATION

BILL OF MATERIALS

Table 5.

Qty	Reference Designator	Description	Manufacturer	Part Number
1	U1	Micropower management unit	Analog Devices, Inc.	ADP5054
1	U2	Dual metal oxide semiconductor field effect transistors, 7.2 mΩ	Infineon	BSC072N03
4	CIN_1, CIN_2, CIN_3, CIN_4	Multilayer ceramic chip capacitor, 10 µF, 25 V, 0805	Murata	GRM219R61E106KA12L
6	COUT_1, COUT_2, COUT_3, COUT_5, COUT_6, COUT_8	Multilayer ceramic chip capacitor, 47 µF, 6.3 V, 0805	Murata	GRM21BR60J476ME15
2	COUT_9, COUT_10, COUT_13, COUT_14	Multilayer ceramic chip capacitor, 47 µF, 6.3 V, 0805	Murata	GRM21BR60J476ME15
1	L1	Inductor, 1.2 µH, 12.5 A	Coilcraft	XAL5030-122ME
1	L2	Inductor, 1.2 µH, 12.5 A	Coilcraft	XAL5030-122ME
1	L3	Inductor, 3.3 µH, 5.5 A	Coilcraft	XAL4030-332ME
1	L4	Inductor, 3.3 µH, 5.5 A	Coilcraft	XAL4030-332ME
5	C1, C3, C4, C5	Multilayer ceramic chip capacitor, 0.1 µF, 16 V, 0402	Murata	GRM155R71C104KA88D
4	C2, C14	Multilayer ceramic chip capacitor, 1 µF, 6.3 V, 0402	Murata	GRM155R60J105KE19D
2	C7, C8	Multilayer ceramic chip capacitor, 1 nF, 50 V, 0402	Murata	GRM155R61H102KA01D
2	C9, C10	Multilayer ceramic chip capacitor, 2.7 nF, 50 V, 0402	Murata	GRM2165C1H272JA01D
1	R2	Resistor, 4.99 kΩ, 1%, 0402	Panasonic	ERJ-2RKF4991X
1	R3	Resistor, 32.4 kΩ, 1%, 0402	Panasonic	ERJ-2RKF2322X
1	R4	Resistor, 12.4 kΩ, 1%, 0402	Vishay	CRCW040231K6F
1	R5	Resistor, 31.2 kΩ, 1%, 0402	Vishay	CRCW040252K3F
1	R6	Resistor, 8.75 kΩ, 1%, 0402	Panasonic	ERJ-2RKF1242X
2	R7, R8	Resistor, 22 kΩ, 1%, 0402	Panasonic	ERJ-2GEJ223X
1	R17	Resistor, 20 kΩ, 1%, 0402	Panasonic	ERJ-2RKF2002X
2	R12, R15	Resistor, 10 kΩ, 1%, 0603	Vishay	CRCW060310K0F
1	R20	Resistor, 51 kΩ, 1%, 0402	Panasonic	ERJ-2RKF2402
2	R39, R40	Resistor, 0 Ω, 1%, 0402	Panasonic	ERJ-2GE0R00X
2	D2	LED, 0603	Panasonic	LNJ208R8ARA
5	J-EN1, J-EN2, J-EN3, J-EN4, J-SYNC	3-pin header	Samtec	TSW-103-08-G-S
15	J11, J12, J15, J16, J17, J18, J19, J20, J21, J22, S1, S2, S3, S4, S5	2-pin header	Samtec	TSW-150-07-T-S
8	TP9, TP10, TP11, VREG, PWRGD_A0	Test point, 1206	MAC8	HK-1-G
6	COUT_4, COUT_11, COUT_12, COUT_15, COUT_7, COUT_16	No assembly	No assembly	No assembly

RELATED LINKS

Resource	Description
ADP5054	4-channel integrated power solution with quad buck regulator

NOTES

ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

ANALOG DEVICES

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