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Cypress (NASDAQ: CY) delivers high-performance, high-quality solutions at the heart of today's most advanced embedded systems, from automotive, industrial and networking platforms to highly interactive consumer and mobile devices. With a broad, differentiated product portfolio that includes NOR flash memories, F-RAM™ and SRAM, Traveo™ microcontrollers, the industry's only PSoC® programmable system-on-chip solutions, analog and PMIC Power Management ICs, CapSense® capacitive touch-sensing controllers, and Wireless BLE Bluetooth® Low-Energy and USB connectivity solutions, Cypress is committed to providing its customers worldwide with consistent innovation, best-in-class support and exceptional system value.

FUJITSU MICROELECTRONICS
DATA SHEET

DS07-16804-3E

32-bit Proprietary Microcontroller

CMOS

FR60Lite MB91210 Series

MB91F211B/213A/F213A/F218S/V210

■ DESCRIPTIONS

MB91210 series is Fujitsu Microelectronics's general-purpose 32-bit RISC microcontroller, which is designed for embedded control applications that require high-speed real-time processing of consumer appliances. This microcontroller uses FR60Lite as its CPU, compatible with other products in the FR* family.

This series incorporates a built-in UART with LIN function and CAN controller.

* : FR, the abbreviation of FUJITSU RISC controller, is a line of products of Fujitsu Microelectronics Limited.

■ FEATURES

- FR CPU
  - 32-bit RISC, load/store architecture, 5-stage pipeline
  - Maximum operating frequency : 40 MHz (Source oscillation is 4 MHz - PLL clock multiplier system)
  - 16-bit fixed length instructions (basic instructions), one instruction per cycle
  - Memory-memory transfer instructions, bit processing instructions, barrel shift instructions
    - Instructions adapted for embedded applications
  - Function entry/exit instructions, multiple-register load/store instructions
    - Instructions supporting high-level language
  - Register interlock function
    - Easier assembler coding enabled
  - Built-in multiplier supported at the instruction level
    - Signed 32-bit multiplication: 5 cycles
    - Signed 16-bit multiplication: 3 cycles
  - Interrupt (PC/PS save) : 6 cycles, 16 priority levels
  - Harvard architecture allowing program access and data access to be executed simultaneously.
  - Instruction compatible with the FR family

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For the information for microcontroller supports, see the following web site.
This web site includes the **"Customer Design Review Supplement"** which provides the latest cautions on system development and the minimal requirements to be checked to prevent problems before the system development.

http://edevice.fujitsu.com/micom/en-support/

2009.2

- Internal ROM size & ROM type
  - Mask ROM : 544 Kbytes (MB91213A)
  - Flash Memory : 288 Kbytes (MB91F211B)
    : 544 Kbytes (MB91F213A/F218S)
- Internal RAM size : 24 Kbytes (MB91213A/F213A/F218S)
  : 16 Kbytes (MB91F211B)
- DMA Controller
  - Capable of simultaneous operation of up to 5 channels
  - Two transfer sources (internal peripheral/software)
- Bit Search Module (for REALOS)
  - Search for the position of the first bit that changes from “1” to “0” in one word, from the MSB
- UART with LIN function (7 channels)
  - Asynchronous clock communication (start-stop synchronization), synchronous clock communication
  - Synch-Break detection
  - Dedicated built-in baud-rate generator for each channel
  - SPI compliant (Mode 2 : clock synchronous communication mode)
- CAN Controller (3 channels)
  - Maximum transfer rate : 1 Mbps
  - 32 message buffer
- Timers
  - 16-bit reload timer (3 channels)
    Selectable internal clock from 2/8/32 divisions
  - 16-bit free-run timer (4 channels)
  - Output compare (8 channels)
  - Input capture (8 channels)
  - 8/16-bit PPG (16 channels/8 channels)
    Selectable clock source from 1/2/16/64 division of peripheral clock
- Interrupt Controller
  - Interrupts from internal peripherals
  - Priority level can be set by software (16 levels)
- External Interrupt (16 channels)
  - Selectable input from several pins
  - Can be used as CAN WAKEUP
    Noise filter is inserted to CAN WAKEUP (Typ 4 µs)
- A/D Converter (32 channels)
  - 10-bit resolution
  - Sequential comparison
    Conversion time : 3 µs
  - Conversion modes (single conversion mode and scan conversion mode)
  - Activation trigger (software/external trigger/peripheral interrupt)
- Other Interval Timer/Counter
  - 16-bit timebase timer/watchdog timer

(Continued)

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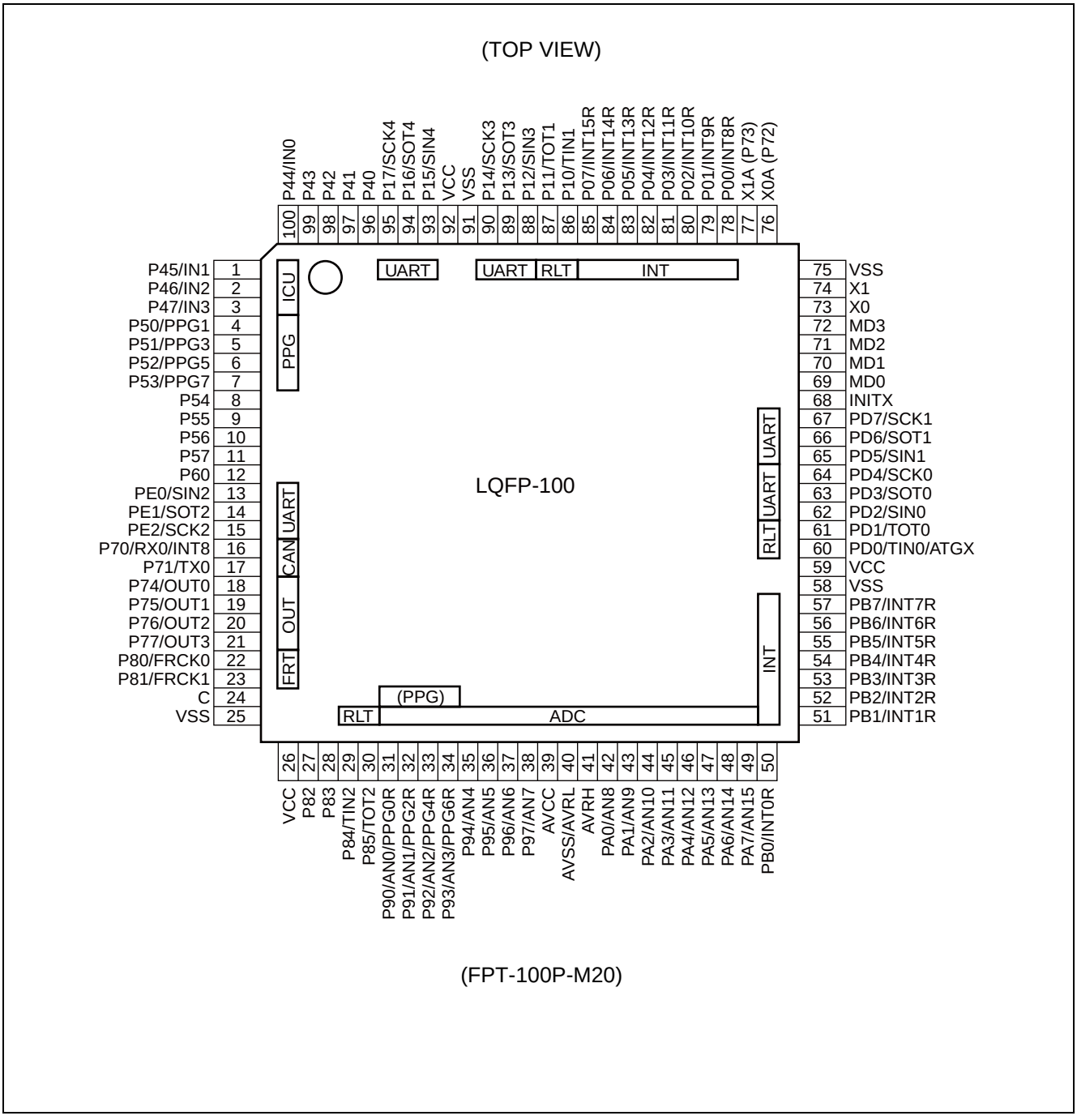
- Other Features
  - Has a built-in oscillation circuit as a clock source, and also can select PLL multiplier
  - INITX is provided as a reset pin
  - Additionally, a watchdog timer reset and software resets are provided
  - Stop mode, sleep mode and real time clock mode supported as low-power consumption modes. Low-power operation using 32 kHz CPU operation enabled
  - Gear function
    Clock can be generated from various combinations of PLL multiplier setting (1/2/4/8/10) and division setting (1 to 16) for each clock
  - Built-in timebase timer
  - Package : LQFP-100, LQFP-144
  - CMOS technology (0.18 µm)
  - Power supply voltage : 3.5 V to 5.5 V
    1.8 V is supplied to internal circuit from step-down circuit

- Comparison of Functions

	MB91V210	**MB91F211B**	**MB91F213A**	**MB91213A**	**MB91F218S**
	Evaluation product	**Flash memory product**	**Flash memory product**	**Mask ROM product**	**Flash memory product**
Package	BGA-420	LQFP-100	LQFP-144		
ROM/Flash size	External SRAM	288 Kbytes	544 Kbytes		
RAM size	4 Kbytes + 32 Kbytes	4 Kbytes + 12 Kbytes	4 Kbytes + 20 Kbytes		
External interrupt	16 channels	16 channels	16 channels		
DMA Controller	5 channels	5 channels	5 channels		
External sub-clock	Correspondence	Correspondence	Correspondence		Non-correspondence
Suspected sub-clock	Non-correspondence	Correspondence	Non-correspondence		
RTC	Yes	Yes	Yes		
CAN Controller	3 channels (128 msg/ch)	1 channel (32 msg/ch)	3 channels (32 msg/ch)		
UART with LIN function	7 channels	4 channels (LIN corresponding) 1 channel (LIN non-corresponding)	7 channels		
Reload Timer	3 channels	3 channels	3 channels		
Free-run timer	4 channels	2 channels	4 channels		
ICU	8 channels	4 channels	8 channels		
OUT	8 channels	4 channels	8 channels		
8/16bits PPG	8bits × 16 channels (16bits × 8 channels)	8bits × 8 channels (16bits × 4 channels)	8bits × 16 channels (16bits × 8 channels)		
A/D Converter	32 channels	16 channels	32 channels		

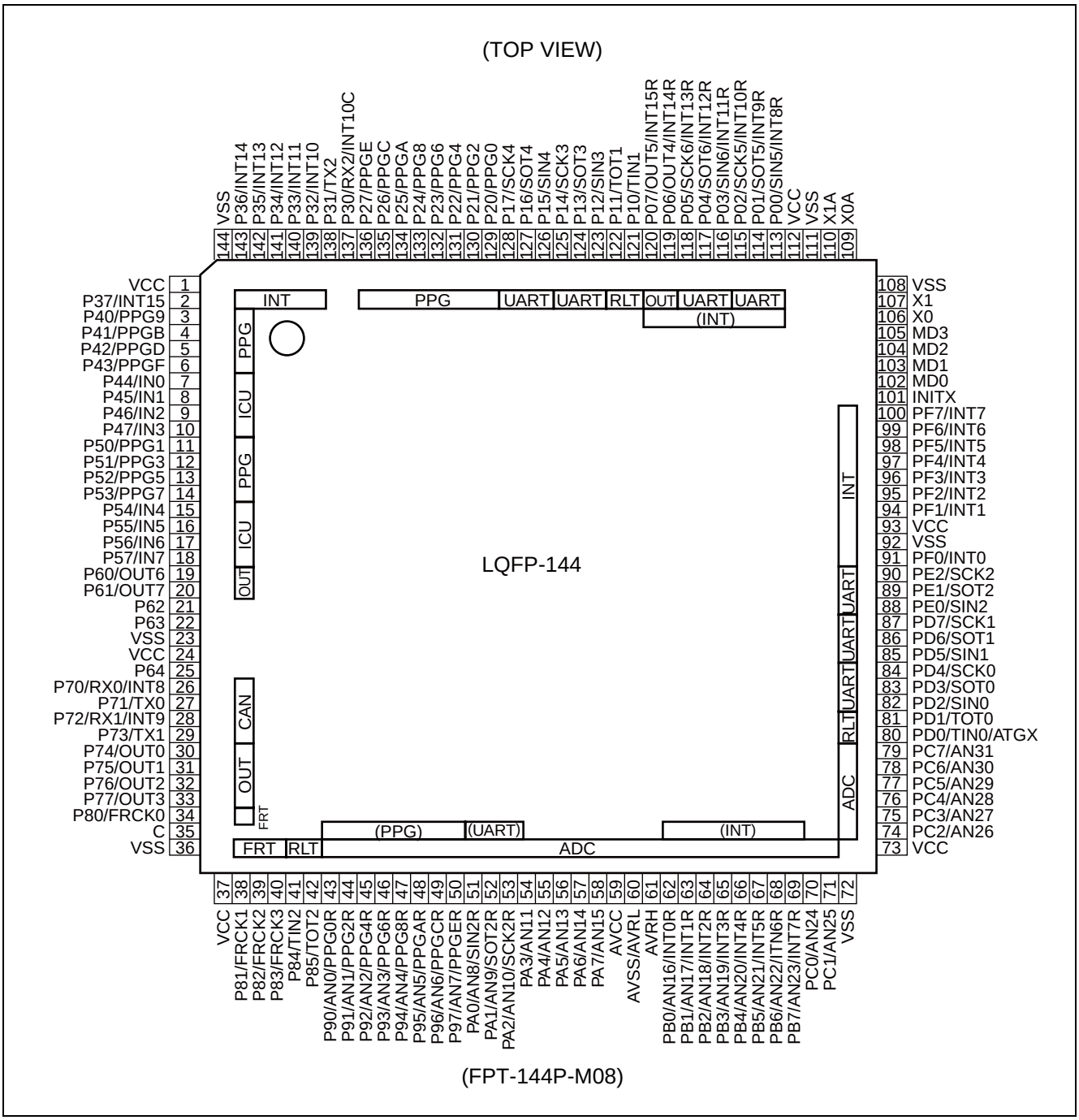
■ PIN ASSIGNMENT

•MB91F211B



(FPT-100P-M20)

•MB91213A/F213A/F218S



■ PIN DESCRIPTIONS

• Pin Functions

Pin no.		Pin name	Function name	I/O circuit type*3	Function
LQFP*1	LQFP*2				
73	106	X0	X0	OA OB	Oscillator input pin
74	107	X1	X1		Oscillator output pin
68	101	INITX	INITX	D	System reset input pin
72	105	MD3	MD3	E	Operation mode input pin
71 to 69	104 to 102	MD2 to MD0	MD2 to MD0	C	Operation mode input pins
76	109	X0A	X0A	WA WB	Sub-oscillation input pin
77	110	X1A	X1A		Sub-oscillation output pin
78	113	P00	P00	A	General purpose I/O port
			SIN5*5		UART5 data input
			INT8R		External interrupt 8 input (select with P70)
79	114	P01	P01	A	General purpose I/O port
			SOT5*5		UART5 data output
			INT9R		External interrupt 9 input (select with P72)
80	115	P02	P02	A	General purpose I/O port
			SCK5*5		UART5 clock I/O
			INT10R		External interrupt 10 input (select with P32)
81	116	P03	P03	A	General purpose I/O port
			SIN6*5		UART6 data input
			INT11R		External interrupt 11 input (select with P33)
82	117	P04	P04	A	General purpose I/O port
			SOT6*5		UART6 data output
			INT12R		External interrupt 12 input (select with P34)
83	118	P05	P05	A	General purpose I/O port
			SCK6*5		UART6 clock I/O
			INT13R		External interrupt 13 input (select with P35)
84	119	P06	P06	A	General purpose I/O port
			OUT4*5		OUT4 output
			INT14R		External interrupt 14 input (select with P36)
85	120	P07	P07	A	General purpose I/O port
			OUT5*5		OUT5 output
			INT15R		External interrupt 15 input (select with P37)
86	121	P10	P10	A	General purpose I/O port
			TIN1		External event input of reload timer 1

(Continued)

Pin no.		Pin name	Function name	I/O circuit type*3	Function
LQFP*1	LQFP*2				
87	122	P11	P11	A	General purpose I/O port
			TOT1		Reload timer 1 output
88	123	P12	P12	A	General purpose I/O port
			SIN3		UART3 data input
89	124	P13	P13	A	General purpose I/O port
			SOT3		UART3 data output
90	125	P14	P14	A	General purpose I/O port
			SCK3		UART3 clock I/O
93	126	P15	P15	A	General purpose I/O port
			SIN4		UART4 data input
94	127	P16	P16	A	General purpose I/O port
			SOT4		UART4 data output
95	128	P17	P17	A	General purpose I/O port
			SCK4		UART4 clock I/O
—	129	P20	P20	A	General purpose I/O port
			PPG0		PPG0 output
—	130	P21	P21	A	General purpose I/O port
			PPG2		PPG2 output
—	131	P22	P22	A	General purpose I/O port
			PPG4		PPG4 output
—	132	P23	P23	A	General purpose I/O port
			PPG6		PPG6 output
—	133	P24	P24	A	General purpose I/O port
			PPG8		PPG8 output
—	134	P25	P25	A	General purpose I/O port
			PPGA		PPGA output
—	135	P26	P26	A	General purpose I/O port
			PPGC		PPGC output
—	136	P27	P27	A	General purpose I/O port
			PPGE		PPGE output
—	137	P30	P30	A	General purpose I/O port
			RX2		CAN2 input
			INT10C		External interrupt 10 input (select with P32)
—	138	P31	P31	A	General purpose I/O port
			TX2		CAN2 output

(Continued)

Pin no.		Pin name	Function name	I/O circuit type*3	Function
LQFP*1	LQFP*2				
—	139	P32	P32	A	General purpose I/O port
			INT10		External interrupt 10 input (select with P30)
—	140	P33	P33	A	General purpose I/O port
			INT11		External interrupt 11 input (select with P03)
—	141	P34	P34	A	General purpose I/O port
			INT12		External interrupt 12 input (select with P04)
—	142	P35	P35	A	General purpose I/O port
			INT13		External interrupt 13 input (select with P05)
—	143	P36	P36	A	General purpose I/O port
			INT14		External interrupt 14 input (select with P06)
—	2	P37	P37	A	General purpose I/O port
			INT15		External interrupt 15 input (select with P07)
96	3	P40	P40	A	General purpose I/O port
			PPG9*5		PPG9 output
97	4	P41	P41	A	General purpose I/O port
			PPGB*5		PPGB output
98	5	P42	P42	A	General purpose I/O port
			PPGD*5		PPGD output
99	6	P43	P43	A	General purpose I/O port
			PPGF*5		PPGF output
100	7	P44	P44	A	General purpose I/O port
			IN0		ICU0 input
1	8	P45	P45	A	General purpose I/O port
			IN1		ICU1 input
2	9	P46	P46	A	General purpose I/O port
			IN2		ICU2 input
3	10	P47	P47	A	General purpose I/O port
			IN3		ICU3 input
4	11	P50	P50	A	General purpose I/O port
			PPG1		PPG1 output
5	12	P51	P51	A	General purpose I/O port
			PPG3		PPG3 output
6	13	P52	P52	A	General purpose I/O port
			PPG5		PPG5 output

(Continued)

Pin no.		Pin name	Function name	I/O circuit type*3	Function
LQFP*1	LQFP*2				
7	14	P53	P53	A	General purpose I/O port
			PPG7		PPG7 output
8	15	P54	P54	A	General purpose I/O port
			IN4*5		ICU4 input
9	16	P55	P55	A	General purpose I/O port
			IN5*5		ICU5 input
10	17	P56	P56	A	General purpose I/O port
			IN6*5		ICU6 input
11	18	P57	P57	A	General purpose I/O port
			IN7*5		ICU7 input
12	19	P60	P60	A	General purpose I/O port
			OUT6*5		OUT6 output
—	20	P61	P61	A	General purpose I/O port
			OUT7		OUT7 output
—	21	P62	P62	A	General purpose I/O port
—	22	P63	P63	A	General purpose I/O port
—	25	P64	P64	A	General purpose I/O port
16	26	P70	P70	A	General purpose I/O port
			RX0		CAN0 input
			INT8		External interrupt 8 input (select with P00)
17	27	P71	P71	A	General purpose I/O port
			TX0		CAN0 output
(76) *4	28	P72	P72	A	General purpose I/O port
			RX1		CAN1 input
			INT9		External interrupt 9 input (select with P01)
(77) *4	29	P73	P73	A	General purpose I/O port
			TX1		CAN1 output
18	30	P74	P74	A	General purpose I/O port
			OUT0		OUT0 output
19	31	P75	P75	A	General purpose I/O port
			OUT1		OUT1 output
20	32	P76	P76	A	General purpose I/O port
			OUT2		OUT2 output
21	33	P77	P77	A	General purpose I/O port
			OUT3		OUT3 output

(Continued)

Pin no.		Pin name	Function name	I/O circuit type*3	Function
LQFP*1	LQFP*2				
22	34	P80	P80	A	General purpose I/O port
			FRCK0		External clock input of free-run timer 0
23	38	P81	P81	A	General purpose I/O port
			FRCK1		External clock input of free-run timer 1
27	39	P82	P82	A	General purpose I/O port
			FRCK2*5		External clock input of free-run timer 2
28	40	P83	P83	A	General purpose I/O port
			FRCK3*5		External clock input of free-run timer 3
29	41	P84	P84	A	General purpose I/O port
			TIN2		External event input of reload timer 2
30	42	P85	P85	A	General purpose I/O port
			TOT2		Reload timer 2 output
31	43	P90	P90	B	General purpose I/O port
			AN0		A/D converter analog input
			PPG0R		PPG0 output (select with P20)
32	44	P91	P91	B	General purpose I/O port
			AN1		A/D converter analog input
			PPG2R		PPG2 output (select with P21)
33	45	P92	P92	B	General purpose I/O port
			AN2		A/D converter analog input
			PPG4R		PPG4 output (select with P22)
34	46	P93	P93	B	General purpose I/O port
			AN3		A/D converter analog input
			PPG6R		PPG6 output (select with P23)
35	47	P94	P94	B	General purpose I/O port
			AN4		A/D converter analog input
			PPG8R*5		PPG8 output (select with P24)
36	48	P95	P95	B	General purpose I/O port
			AN5		A/D converter analog input
			PPGAR*5		PPGA output (select with P25)
37	49	P96	P96	B	General purpose I/O port
			AN6		A/D converter analog input
			PPGCR*5		PPGC output (select with P26)

(Continued)

Pin no.		Pin name	Function name	I/O circuit type*3	Function
LQFP*1	LQFP*2				
38	50	P97	P97	B	General purpose I/O port
			AN7		A/D converter analog input
			PPGER*5		PPGE output (select with P27)
42	51	PA0	PA0	B	General purpose I/O port
			AN8		A/D converter analog input
			SIN2R*5		UART2 data input (select with PE0)
43	52	PA1	PA1	B	General purpose I/O port
			AN9		A/D converter analog input
			SOT2R*5		UART2 data output (select with PE1)
44	53	PA2	PA2	B	General purpose I/O port
			AN10		A/D converter analog input
			SCK2R*5		UART2 clock I/O (select with PE2)
45	54	PA3	PA3	B	General purpose I/O port
			AN11		A/D converter analog input
46	55	PA4	PA4	B	General purpose I/O port
			AN12		A/D converter analog input
47	56	PA5	PA5	B	General purpose I/O port
			AN13		A/D converter analog input
48	57	PA6	PA6	B	General purpose I/O port
			AN14		A/D converter analog input
49	58	PA7	PA7	B	General purpose I/O port
			AN15		A/D converter analog input
50	62	PB0	PB0	B	General purpose I/O port
			AN16*5		A/D converter analog input
			INT0R		External interrupt 0 input (select with PF0)
51	63	PB1	PB1	B	General purpose I/O port
			AN17*5		A/D converter analog input
			INT1R		External interrupt 1 input (select with PF1)
52	64	PB2	PB2	B	General purpose I/O port
			AN18*5		A/D converter analog input
			INT2R		External interrupt 2 input (select with PF2)
53	65	PB3	PB3	B	General purpose I/O port
			AN19*5		A/D converter analog input
			INT3R		External interrupt 3 input (select with PF3)

(Continued)

Pin no.		Pin name	Function name	I/O circuit type*3	Function
LQFP*1	LQFP*2				
54	66	PB4	PB4	B	General purpose I/O port
			AN20*5		A/D converter analog input
			INT4R		External interrupt 4 input (select with PF4)
55	67	PB5	PB5	B	General purpose I/O port
			AN21*5		A/D converter analog input
			INT5R		External interrupt 5 input (select with PF5)
56	68	PB6	PB6	B	General purpose I/O port
			AN22*5		A/D converter analog input
			INT6R		External interrupt 6 input (select with PF6)
57	69	PB7	PB7	B	General purpose I/O port
			AN23*5		A/D converter analog input
			INT7R		External interrupt 7 input (select with PF7)
—	70	PC0	PC0	B	General purpose I/O port
			AN24		A/D converter analog input
—	71	PC1	PC1	B	General purpose I/O port
			AN25		A/D converter analog input
—	74	PC2	PC2	B	General purpose I/O port
			AN26		A/D converter analog input
—	75	PC3	PC3	B	General purpose I/O port
			AN27		A/D converter analog input
—	76	PC4	PC4	B	General purpose I/O port
			AN28		A/D converter analog input
—	77	PC5	PC5	B	General purpose I/O port
			AN29		A/D converter analog input
—	78	PC6	PC6	B	General purpose I/O port
			AN30		A/D converter analog input
—	79	PC7	PC7	B	General purpose I/O port
			AN31		A/D converter analog input
60	80	PD0	PD0	A	General purpose I/O port
			TIN0		External event input of reload timer 0
			ATGX		A/D converter external trigger input
61	81	PD1	PD1	A	General purpose I/O port
			TOT0		Reload timer 0 output
62	82	PD2	PD2	A	General purpose I/O port
			SIN0		UART0 data input

(Continued)

Pin no.		Pin name	Function name	I/O circuit type*3	Function
LQFP*1	LQFP*2				
63	83	PD3	PD3	A	General purpose I/O port
			SOT0		UART0 data output
64	84	PD4	PD4	A	General purpose I/O port
			SCK0		UART0 clock I/O
65	85	PD5	PD5	A	General purpose I/O port
			SIN1		UART1 data input
66	86	PD6	PD6	A	General purpose I/O port
			SOT1		UART1 data output
67	87	PD7	PD7	A	General purpose I/O port
			SCK1		UART1 clock I/O
13	88	PE0	PE0	A	General purpose I/O port
			SIN2		UART2 data input
14	89	PE1	PE1	A	General purpose I/O port
			SOT2		UART2 data output
15	90	PE2	PE2	A	General purpose I/O port
			SCK2		UART2 clock I/O
—	91	PF0	PF0	A	General purpose I/O port
			INT0		External interrupt 0 input
—	94	PF1	PF1	A	General purpose I/O port
			INT1		External interrupt 1 input
—	95	PF2	PF2	A	General purpose I/O port
			INT2		External interrupt 2 input
—	96	PF3	PF3	A	General purpose I/O port
			INT3		External interrupt 3 input
—	97	PF4	PF4	A	General purpose I/O port
			INT4		External interrupt 4 input
—	98	PF5	PF5	A	General purpose I/O port
			INT5		External interrupt 5 input
—	99	PF6	PF6	A	General purpose I/O port
			INT6		External interrupt 6 input
—	100	PF7	PF7	A	General purpose I/O port
			INT7		External interrupt 7 input
26, 59, 92	1, 24, 37, 73, 93, 112	VCC	—	—	Power supply pins (5 V)

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Pin no.		Pin name	Function name	I/O circuit type*3	Function
LQFP*1	LQFP*2				
25, 58, 75, 91	23, 36, 72, 92, 108, 111, 144	VSS	—	—	Power supply pins (0 V)
24	35	C	—	—	Power stabilization capacitance pin
39	59	AVCC	—	—	Analog power supply pin
40	60	AVSS	—	—	Analog power supply pin
		AVRL	—	—	Base power supply pin for A/D converter
41	61	AVRH	—	—	Base power supply pin for A/D converter

*1 : FPT-100P-M20

*2 : FPT-144P-M08

*3 : For information about the I/O circuit type, refer to “ ■ I/O CIRCUIT TYPE”.

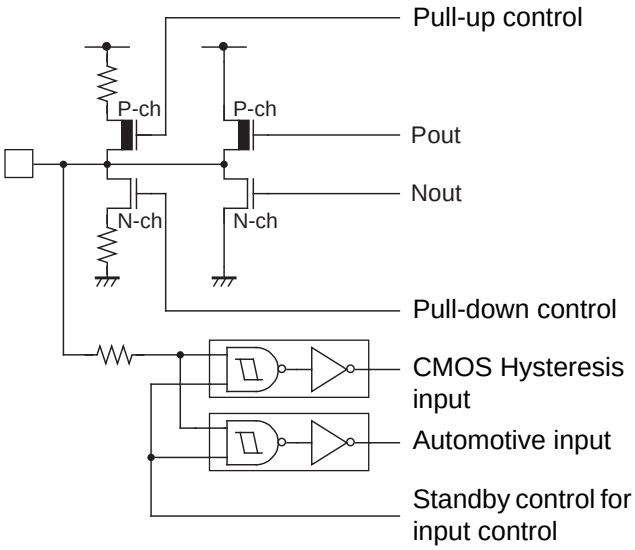
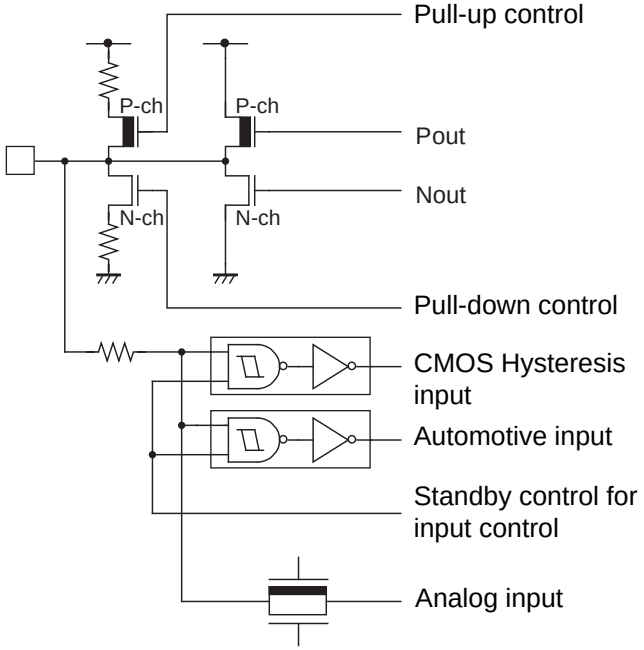
*4 : MB91F211B can be selected by MD3 to MD0 of mode pins.

*5 : Only MB91213A/F213A/F218S

MD pin	76 pin	77 pin
0000	X0A	X1A
0011	P72	P73
Other than above	Setting prohibited	

P72 and P73 function as general-purpose I/O ports only.

■ I/O CIRCUIT TYPE

Group	Circuit Type	Remarks
A		• CMOS level output • CMOS hysteresis input (with standby-time input shutdown function) • Automotive input (with standby-time input shutdown function)
B		• CMOS level output • CMOS hysteresis input (with standby-time input shutdown function) • Automotive input (with standby-time input shutdown function) • A/D analog input

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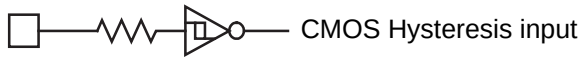
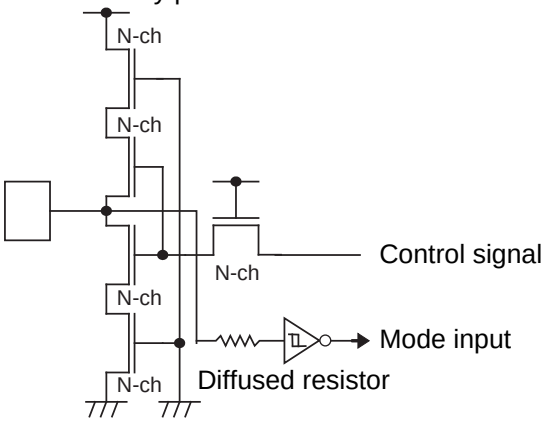
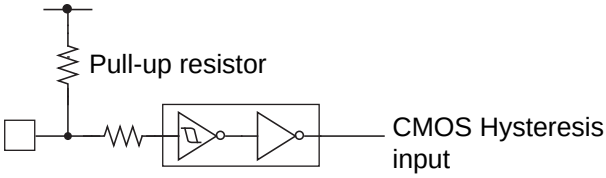
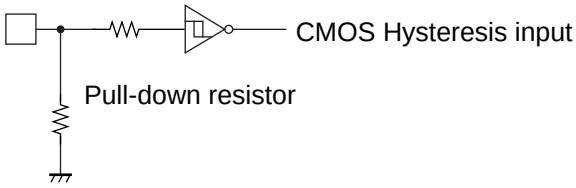
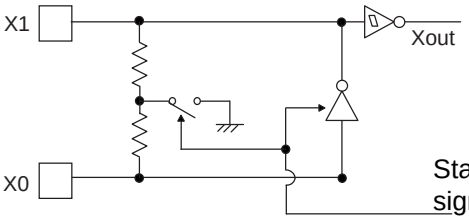
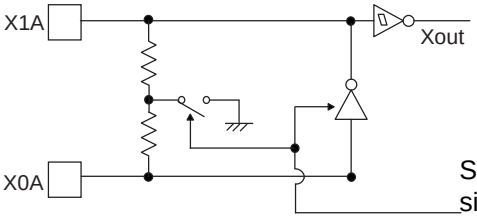
(Continued)

Group	Circuit Type	Remarks
C	Mask ROM product  CMOS Hysteresis input Flash memory product  N-ch N-ch N-ch N-ch N-ch Control signal Mode input Diffused resistor	Mask ROM product • CMOS hysteresis input • MD 2 : Pull-down provided Flash memory product • High-voltage control signal for test provided • MD 2 : No pull-down provided
D	 Pull-up resistor CMOS Hysteresis input	CMOS hysteresis input
E	 CMOS Hysteresis input Pull-down resistor	CMOS hysteresis input
OA OB	 X1 Xout X0 Standby control signal	Oscillation circuit High speed oscillation feedback resistance : approx. 1 MΩ
WA WB	 X1A Xout X0A Standby control signal	Oscillation circuit Low speed oscillation feedback resistance : approx. 20 MΩ (MB91213A/F213A/F218S/V210) approx. 10MΩ (MB91F211B)

■ HANDLING DEVICES

• Preventing latch-up

Latch-up may occur in a CMOS IC, if a voltage greater than VCC pin or less than VSS pin is applied to input and output pin, or if an above-rating voltage is applied between V_{CC} and V_{SS}. When latch-up occurs, it may significantly increase the power supply current, and may cause thermal destruction of an element. When you use a CMOS IC, be very careful not to exceed the maximum rating.

• Treatment of unused pins

Do not leave an unused input pin open, since it may cause a malfunction. Handle by performing a pull-up or pull-down with a resistance of 2 kΩ or more. An unused I/O pin should be set to the output status and left open. When set to the input status, it should be handled in the same way as an input pin.

• Serial Communication

There is a possibility to receive wrong data due to the noise or other causes on the serial communication.
Therefore, design a printed circuit board so as to avoid noise.
Retransmit the data if an error occurs because of applying the checksum to the last data in consideration of receiving wrong data due to the noise.

• About power supply pins

If there are multiple VCC and VSS pins, from the point of view of device design pins to be of the same potential are connected inside the device to prevent such malfunctioning as latch-up. However, you must connect all the pins to external power supply and a ground line to lower the electro-magnetic emission level, to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total output current rating. Moreover, connect the current supply source with the VCC and VSS pins of this device at the low impedance.

Furthermore, it is also advisable to connect a ceramic bypass capacitor of approximately 0.1 µF between VCC and VSS pins near this device.

This device incorporates a regulator. When using the device with 5 V power supply, apply that power supply to the VCC pin and always connect a 1 µF or greater capacitor to the C pin for the regulator.

• Crystal oscillator circuit

Noise near the X0/X1 pins and X0A/X1A pins may cause the device to malfunction. Design the PC board such that X0/X1 pins, X0A/X1A pins, the crystal oscillator (or ceramic oscillator), and the bypass capacitor to the ground are placed as near one another as possible. When routing the X0 and X1 signals, they should be shielded for use on the board. Caution must be taken especially when using a pin next to the X0.

It is strongly recommended to design the PC board artwork with the X0, X1, X0A and X1A pins surrounded by ground plane because stable operation can be expected with such a layout.

In addition, a sub clock is required even when a dual clock product is used as a single clock product.

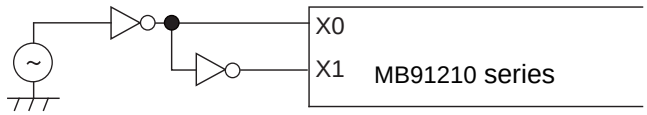
For MB91F218S input "L" level to X0A pin and open X1A pin.

Please ask the crystal maker to evaluate the oscillational characteristics of the crystal and this device.

- Notes on using external clock

  When an external clock is used, supply the opposite phase clock to X0/X1 pins, simultaneously. Note that input only to X0 pin cannot be used. Also, when an external clock is used, do not use the STOP mode (oscillation stop mode). (This is because the X1 pin stops at “H” output in the STOP mode.)

Example Application of External Clock (Normal)



Note : STOP mode (oscillation stop mode) cannot be used.

- Handling of NC/OPEN pins

  Always leave NC pins and OPEN pins open.

- Mode pins (MD0 to MD3)

  These pins should be connected directly to VCC or VSS pins. To prevent the device erroneously switching to test mode due to noise, design the PC board such that the distance between the mode pins and VCC or VSS pins is as short as possible and the connection impedance is now.

  MD3 pin must be connected to VSS pin directly with a resistance of 0 Ω.

- Power-on

  Upon power-on, INITX pin must have been set to “L” level.

- Source oscillation input upon power-on

  Upon power-on, never fail to input the clock until the oscillation stabilization wait is cancelled.

- About Flash write

  Note that Flash write/erase is not possible in the sub mode.

- Treatment of power supply pins on A/D converter

  Connect to ensure “$AV_{CC} = V_{CC}$ and $AV_{SS} = V_{SS}$” even if the A/D converter is not in use.

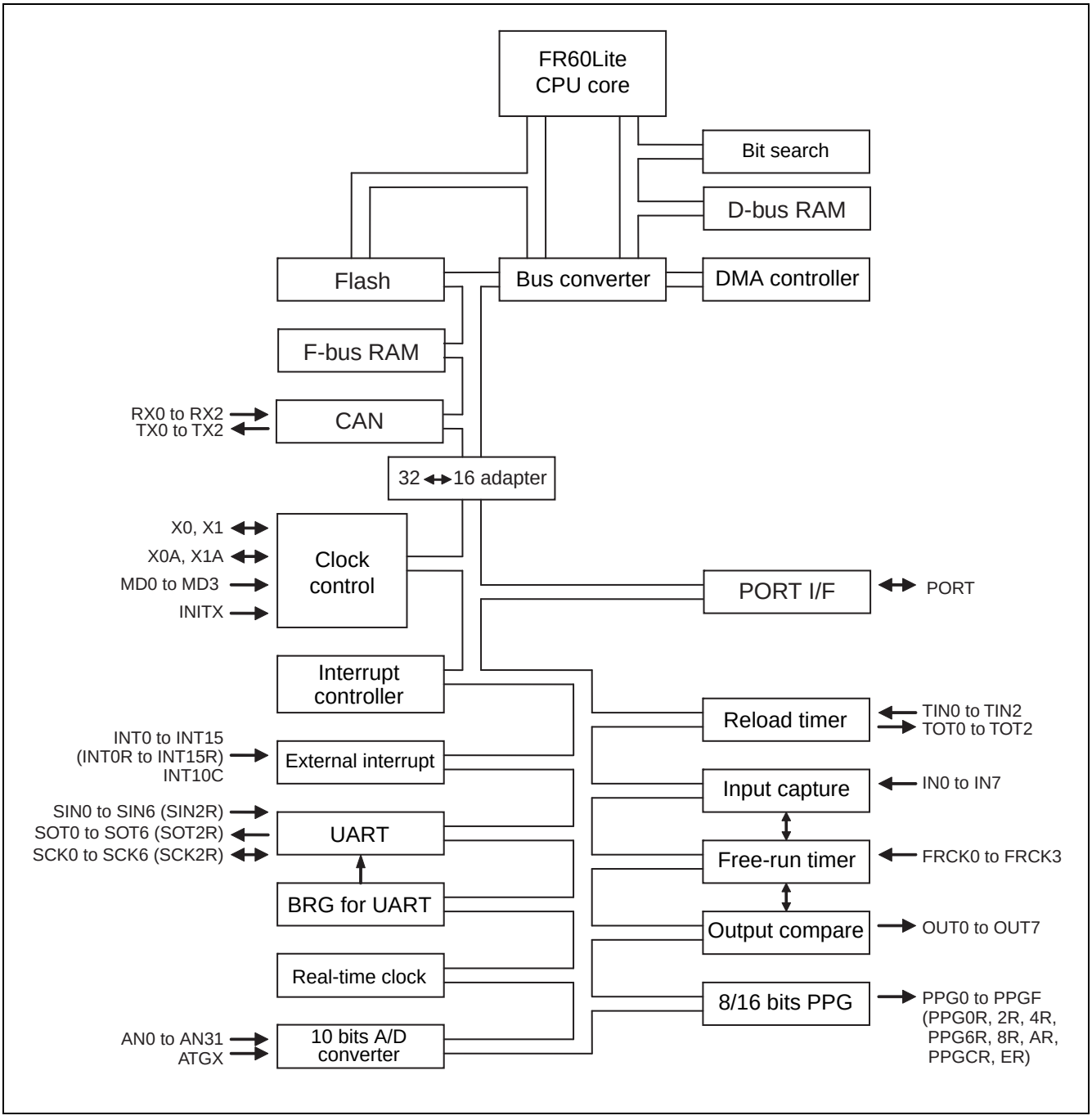
- Power-on sequence for power supply analog input of A/D converter

  Always supply power to the A/D converter (AV_{CC} and AVRH) and apply analog input (AN0 to AN 31) after turning on the digital power supply (V_{CC}). Also, turn off the power supply for the A/D converter and analog input before turning off the digital power supply (V_{CC}). In so doing, the power supply must be turn on and off so that AVRH does not exceed AV_{CC}. Even when using a pin shared with analog input as an input port, ensure that the input voltage does not exceed AV_{CC} (There is no problem in turning on or off the A/D converter (AV_{CC} and AVRH) and digital power supplies at the same time).

- Caution on operations during PLL clock mode

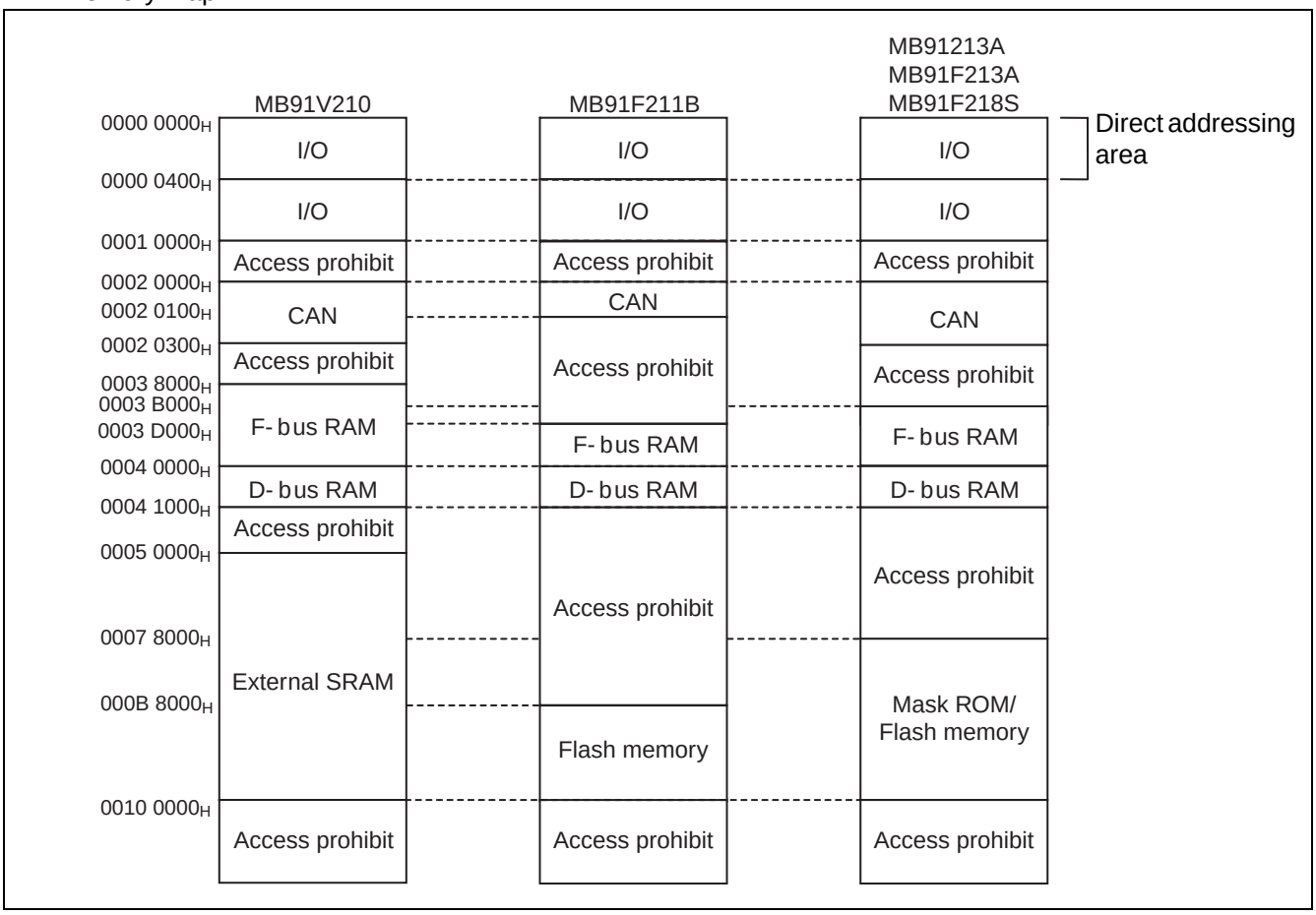
  Even if the oscillator comes off or the clock input stops with the PLL clock selected for this microcontroller, the microcontroller may continue to operate at the free-running frequency of the PLL’s internal self-oscillating oscillator circuit. Performance of this operation is not guaranteed.

■ BLOCK DIAGRAM



■ MEMORY SPACE

• Memory map



■ MODE SETTINGS

In the FR family, the operating mode is set by the mode pins (MD3, 2, 1, 0) and the mode register (MODR).

• Mode pins

There are four mode pins (MD3 to MD0) to specify how to fetch the mode vector.

Settings other than these in the table are prohibited.

Mode pin				Mode name	Reset vector access area	Remarks
MD3	MD2	MD1	MD0			
0	0	0	0	Internal ROM mode vector	Internal	
0	0	0	1	External ROM mode vector	External	Setting is prohibited in this device.

Note: In the FR family, the external mode vector fetch by a multiplex bus is not supported.

• Mode data

Data written to the mode register by a mode vector fetch is called mode data.

After an operating mode has been set in the mode register (MODR), the device operates in that operating mode.

The mode data is set by all reset sources. User programs cannot set data to the mode register.

Detailed description of mode data

[bit7 to bit3] Reserved bits

Always set the value to “00000_B”.

Normal operation is not guaranteed when a value other than “00000_B” is set.

[bit2] ROMA (Internal ROM enable bit)

This bit sets whether to enable F-bus ROM areas.

ROMA	Function	Remarks
0	External ROM mode	Internal ROM area (50000_H to $FFFFF_H$) becomes the external area.
1	Internal ROM mode	F-bus ROM is enabled.

[bit1, bit0] WTH1, WTH0 (Bus width specification bits)

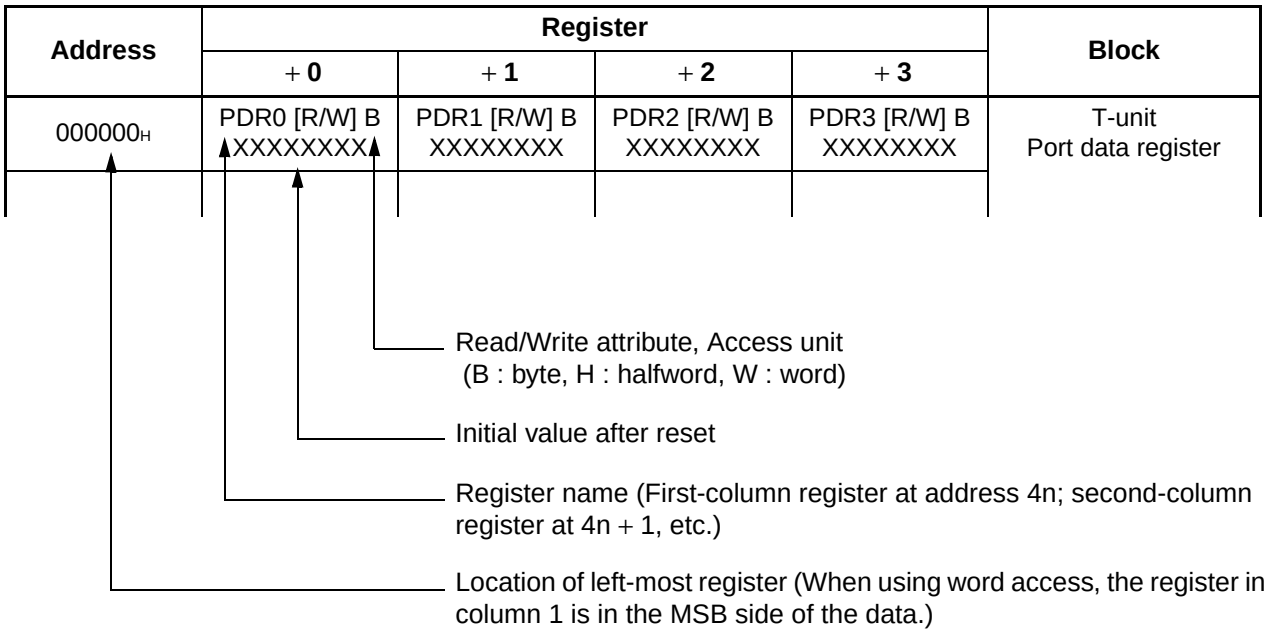
These bits set the bus width specification in external bus mode.

In external bus mode, this value is set in the DBW0 bit of ACR0 (CS0 area).

WTH1	WTH0	Function	Remarks
0	0	8-bit bus width	Setup prohibited
0	1	16-bit bus width	Setup prohibited
1	0	—	Setup prohibited
1	1	Single-chip mode	Single-chip mode

■ I/O MAP

[How to read the map]



Notes: Initial values of register bits are represented as follows :

- “1” : Initial value “1”
- “0” : Initial value “0”
- “X” : Initial value “undefined”
- “-” : No physical register present at this location.

Access by any undescribed data is prohibited.

Address	Register				Block
	+0	+1	+2	+3	
000000H	PDR0 (R/W) B, H, W XXXXXXXX	PDR1 (R/W) B, H, W XXXXXXXX	PDR2 (R/W) B, H, W XXXXXXXX	PDR3 (R/W) B, H, W XXXXXXXX	Port Data Register
000004H	PDR4 (R/W) B, H, W XXXXXXXX	PDR5 (R/W) B, H, W XXXXXXXX	PDR6 (R/W) B, H, W ---XXXXX	PDR7 (R/W) B, H, W XXXXXXXX	
000008H	PDR8 (R/W) B, H, W --XXXXXX	PDR9 (R/W) B, H, W XXXXXXXX	PDRA (R/W) B, H, W XXXXXXXX	PDRB (R/W) B, H, W XXXXXXXX	
00000CH	PDRC (R/W) B, H, W XXXXXXXX	PDRD (R/W) B, H, W XXXXXXXX	PDRE (R/W) B, H, W -----XXX	PDRF (R/W) B, H, W XXXXXXXX	
000010H to 00003CH	—	—	—	—	Reserved
000040H	EIRR0 (R/W) B, H, W 00000000	ENIR0 (R/W) B, H, W 00000000	ELVR0 (R/W) B, H, W 00000000 00000000		External interrupt (INT0 to INT7)
000044H	DICR (R/W) B, H, W -------0	HRCL (R/W, R) B 0--11111	—		Delay interrupt module/ Hold Request
000048H	TMRLR0 (W) H, W XXXXXXXX XXXXXXXX		TMR0 (R) H, W XXXXXXXX XXXXXXXX		Reload timer 0
00004CH	—	—	TMCSR0 (R/W, R) B, H, W ----0000 00000000		
000050H	TMRLR1 (W) H, W XXXXXXXX XXXXXXXX		TMR1 (R) H, W XXXXXXXX XXXXXXXX		Reload timer 1
000054H	—	—	TMCSR1 (R/W, R) B, H, W ----0000 00000000		
000058H	TMRLR2 (W) H, W XXXXXXXX XXXXXXXX		TMR2 (R) H, W XXXXXXXX XXXXXXXX		Reload timer 2
00005CH	—	—	TMCSR2 (R/W, R) B, H, W ----0000 00000000		
000060H	SCR0 (R/W, W) B, H, W 00000000	SMR0 (R/W, W) B, H, W 00000000	SSR0 (R/W, R) B, H, W 00001000	RDR0/TDR0 (R/W) B, H, W 00000000	UART 0
000064H	ESCR0 (R/W) B, H, W 00000100	ECCR0 (R/W, R, W) B, H, W 000000XX	BGR10 (R/W) B, H, W 10000000	BGR00 (R/W) B, H, W 00000000	

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
000068H	SCR5 (R/W, W) B, H, W 00000000	SMR5 (R/W, W) B, H, W 00000000	SSR5 (R/W, R) B, H, W 00001000	RDR5/TDR5 (R/W) B, H, W 00000000	UART 5
00006CH	ESCR5 (R/W) B, H, W 00000100	ECCR5 (R/W, R, W) B, H, W 000000XX	BGR15 (R/W) B, H, W 10000000	BGR05 (R/W) B, H, W 00000000	
000070H	SCR6 (R/W, W) B, H, W 00000000	SMR6 (R/W, W) B, H, W 00000000	SSR6 (R/W, R) B, H, W 00001000	RDR6/TDR6 (R/W) B, H, W 00000000	UART 6
000074H	ESCR6 (R/W) B, H, W 00000100	ECCR6 (R/W, R, W) B, H, W 000000XX	BGR16 (R/W) B, H, W 10000000	BGR06 (R/W) B, H, W 00000000	
000078H to 0000ACH	—	—	—	—	Reserved
0000B0H	SCR1 (R/W, W) B, H, W 00000000	SMR1 (R/W, W) B, H, W 00000000	SSR1 (R/W, R) B, H, W 00001000	RDR1/TDR1 (R/W) B, H, W 00000000	UART 1
0000B4H	ESCR1 (R/W) B, H, W 00000100	ECCR1 (R/W, R, W) B, H, W 000000XX	BGR11 (R/W) B, H, W 10000000	BGR01 (R/W) B, H, W 00000000	
0000B8H	SCR2 (R/W, W) B, H, W 00000000	SMR2 (R/W, W) B, H, W 00000000	SSR2 (R/W, R) B, H, W 00001000	RDR2/TDR2 (R/W) B, H, W 00000000	UART 2
0000BCH	ESCR2 (R/W) B, H, W 00000100	ECCR2 (R/W, R, W) B, H, W 000000XX	BGR12 (R/W) B, H, W 10000000	BGR02 (R/W)B, H, W 00000000	
0000C0H	SCR3 (R/W, W) B, H, W 00000000	SMR3 (R/W, W) B, H, W 00000000	SSR3 (R/W, R) B, H, W 00001000	RDR3/TDR3 (R/W) B, H, W 00000000	UART 3
0000C4H	ESCR3 (R/W) B, H, W 00000100	ECCR3 (R/W, R, W) B, H, W 000000XX	BGR13 (R/W) B, H, W 10000000	BGR03 (R/W) B, H, W 00000000	
0000C8H	SCR4 (R/W, W) B, H, W 00000000	SMR4 (R/W, W) B, H, W 00000000	SSR4 (R/W, R) B, H, W 00001000	RDR4/TDR4 (R/W) B, H, W 00000000	UART 4
0000CCH	ESCR4 (R/W) B, H, W 00000100	ECCR4 (R/W, R, W) B, H, W 000000XX	BGR14 (R/W) B, H, W 10000000	BGR04 (R/W) B, H, W 00000000	
0000D0H	EIRR1 (R/W) B, H, W 00000000	ENIR1 (R/W) B, H, W 00000000	ELVR1 (R/W) B, H, W 00000000 00000000		External interrupt (INT8 to INT15)

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
0000D4H	TCDT0 (R/W) H, W 00000000 00000000		—	TCCS0 (R/W) B, H, W 00000000	Free-run Timer 0
0000D8H	TCDT1 (R/W) H, W 00000000 00000000		—	TCCS1 (R/W) B, H, W 00000000	Free-run Timer 1
0000DCH	TCDT2 (R/W) H, W 00000000 00000000		—	TCCS2 (R/W) B, H, W 00000000	Free-run Timer 2
0000E0H	TCDT3 (R/W) H, W 00000000 00000000		—	TCCS3 (R/W) B, H, W 00000000	Free-run Timer 3
0000E4H	IPCP1 (R) H, W XXXXXXXX XXXXXXXX		IPCP0 (R) H, W XXXXXXXX XXXXXXXX		Input Capture 0, 1
0000E8H	—	—	—	ICS01 (R/W) B, H, W 00000000	
0000ECH	IPCP3 (R) H, W XXXXXXXX XXXXXXXX		IPCP2 (R) H, W XXXXXXXX XXXXXXXX		Input Capture 2, 3
0000F0H	—	—	—	ICS23 (R/W) B, H, W 00000000	
0000F4H	IPCP5 (R) H, W XXXXXXXX XXXXXXXX		IPCP4 (R) H, W XXXXXXXX XXXXXXXX		Input Capture 4, 5
0000F8H	—	—	—	ICS45 (R/W) B, H, W 00000000	
0000FCH	IPCP7 (R) H, W XXXXXXXX XXXXXXXX		IPCP6 (R) H, W XXXXXXXX XXXXXXXX		Input Capture 6, 7
000100H	—	—	—	ICS67 (R/W) B, H, W 00000000	
000104H	—	—	—	—	Reserved
000108H	OCCP1 (R/W) H, W XXXXXXXX XXXXXXXX		OCCP0 (R/W) H, W XXXXXXXX XXXXXXXX		Output Compare 0, 1
00010CH	OCCP3 (R/W) H, W XXXXXXXX XXXXXXXX		OCCP2 (R/W) H, W XXXXXXXX XXXXXXXX		Output Compare 2, 3

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
000110H	OCS23 (R/W) B, H, W 11101100 00001100		OCS01 (R/W) B, H, W 11101100 00001100		Output Compare Cntl 0 to Cntl 3
000114H	OCCP5 (R/W) H, W XXXXXXXX XXXXXXXX		OCCP4 (R/W) H, W XXXXXXXX XXXXXXXX		Output Compare 4, 5
000118H	OCCP7 (R/W) H, W XXXXXXXX XXXXXXXX		OCCP6 (R/W) H, W XXXXXXXX XXXXXXXX		Output Compare 6, 7
00011CH	OCS67 (R/W) B, H, W 11101100 00001100		OCS45 (R/W) B, H, W 11101100 00001100		Output Compare Cntl 4 to Cntl 7
000120H to 000140H	—	—	—	—	Reserved
000144H	—	WTDBL (R/W) B ------00	WTCR (R/W, R) B, H 00000000 000-00-0		Real-time Clock
000148H	—	WTBR2 (R/W) B ---XXXXX	WTBR1 (R/W) B XXXXXXXX	WTBR0 (R/W) B XXXXXXXX	
00014CH	WTHR (R/W) B, H ---XXXXX	WTMR (R/W) B, H --XXXXXX	WTSR (R/W) B --XXXXXX	—	
000150H	ADERH (R/W) B, H, W 00000000 00000000		ADERL (R/W) B, H, W 00000000 00000000		A/D Converter
000154H	ADCS1 (R/W) B, H, W 00000000	ADCS0 (R/W, R) B, H, W 00000000	ADCR1 (R) B, H, W ------XX	ADCR0 (R) B, H, W XXXXXXXX	
000158H	ADCT1 (R/W) B, H, W 00010000	ADCT0 (R/W) B, H, W 00101100	ADSCH (R/W) B, H, W ---00000	ADECH (R/W) B, H, W ---00000	
00015CH	—	CUCR (R/W, R) B, H, W 00000000	CUTD (R/W) B, H, W 10000000 00000000		Sub Clock Calibration unit
000160H	CUTR1 (R) B, H, W 00000000 00000000		CUTR2 (R) B, H, W 00000000 00000000		
000164H to 0001A4H	—	—	—	—	Reserved

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
0001A8H	CANPRE (R/W, R) B, H, W 00000000	—	EISSR (R/W) B, H, W 00000000 00000000		Select CAN Clock Prescaler/external interrupt
0001ACH	—	—	—	—	Reserved
0001B0H	PRLH0 (R/W) B, H, W XXXXXXXX	PRLL0 (R/W) B, H, W XXXXXXXX	PRLH1 (R/W) B, H, W XXXXXXXX	PRLL1 (R/W) B, H, W XXXXXXXX	PPG 0 to PPG 3
0001B4H	PRLH2 (R/W) B, H, W XXXXXXXX	PRLL2 (R/W) B, H, W XXXXXXXX	PRLH3 (R/W) B, H, W XXXXXXXX	PRLL3 (R/W) B, H, W XXXXXXXX	
0001B8H	PPGC0 (R/W) B, H, W 0000000X	PPGC1 (R/W) B, H, W 0000000X	PPGC2 (R/W) B, H, W 0000000X	PPGC3 (R/W) B, H, W 0000000X	
0001BCH	—	—	—	—	Reserved
0001C0H	PRLH4 (R/W) B, H, W XXXXXXXX	PRLL4 (R/W) B, H, W XXXXXXXX	PRLH5 (R/W) B, H, W XXXXXXXX	PRLL5 (R/W) B, H, W XXXXXXXX	PPG 4 to PPG 7
0001C4H	PRLH6 (R/W) B, H, W XXXXXXXX	PRLL6 (R/W) B, H, W XXXXXXXX	PRLH7 (R/W) B, H, W XXXXXXXX	PRLL7 (R/W) B, H, W XXXXXXXX	
0001C8H	PPGC4 (R/W) B, H, W 0000000X	PPGC5 (R/W) B, H, W 0000000X	PPGC6 (R/W) B, H, W 0000000X	PPGC7 (R/W) B, H, W 0000000X	
0001CCH	—	—	—	—	Reserved
0001D0H	PRLH8 (R/W) B, H, W XXXXXXXX	PRLL8 (R/W) B, H, W XXXXXXXX	PRLH9 (R/W) B, H, W XXXXXXXX	PRLL9 (R/W) B, H, W XXXXXXXX	PPG 8 to PPG B
0001D4H	PRLHA (R/W) B, H, W XXXXXXXX	PRLLA (R/W) B, H, W XXXXXXXX	PRLHB (R/W) B, H, W XXXXXXXX	PRLLB (R/W) B, H, W XXXXXXXX	
0001D8H	PPGC8 (R/W) B, H, W 0000000X	PPGC9 (R/W) B, H, W 0000000X	PPGCA (R/W) B, H, W 0000000X	PPGCB (R/W) B, H, W 0000000X	
0001DCH	—	—	—	—	Reserved
0001E0H	PRLHC (R/W) B, H, W XXXXXXXX	PRLLC (R/W) B, H, W XXXXXXXX	PRLHD (R/W) B, H, W XXXXXXXX	PRLLD (R/W) B, H, W XXXXXXXX	PPG C to PPG F
0001E4H	PRLHE (R/W) B, H, W XXXXXXXX	PRLLE (R/W) B, H, W XXXXXXXX	PRLHF (R/W) B, H, W XXXXXXXX	PRLLF (R/W) B, H, W XXXXXXXX	
0001E8H	PPGCC (R/W) B, H, W 0000000X	PPGCD (R/W) B, H, W 0000000X	PPGCE (R/W) B, H, W 0000000X	PPGCF (R/W) B, H, W 0000000X	

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
0001ECH	—	—	—	—	Reserved
0001F0H	TRG1 (R/W) B, H, W 00000000	TRG0 (R/W) B, H, W 00000000	REVC1 (R/W) B, H, W 00000000	REVC0 (R/W) B, H, W 00000000	PPG 0 to PPG F AP/INV
0001F4H to 0001FCH	—	—	—	—	Reserved
000200H	DMACA0 (R/W, R) B, H, W *1 00000000 00000000 00000000 00000000				DMA Controller
000204H	DMACB0 (R/W) B, H, W 00000000 00000000 00000000 00000000				
000208H	DMACA1 (R/W, R) B, H, W *1 00000000 00000000 00000000 00000000				
00020CH	DMACB1 (R/W) B, H, W 00000000 00000000 00000000 00000000				
000210H	DMACA2 (R/W, R) B, H, W *1 00000000 00000000 00000000 00000000				
000214H	DMACB2 (R/W) B, H, W 00000000 00000000 00000000 00000000				
000218H	DMACA3 (R/W, R) B, H, W *1 00000000 00000000 00000000 00000000				
00021CH	DMACB3 (R/W) B, H, W 00000000 00000000 00000000 00000000				
000220H	DMACA4 (R/W, R) B, H, W *1 00000000 00000000 00000000 00000000				
000224H	DMACB4 (R/W) B, H, W 00000000 00000000 00000000 00000000				
000228H to 00023CH	—	—	—	—	Reserved

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
000240H	DMACR (R/W, R) B, H, W 00000000 00000000 00000000 00000000				DMA Controller
000244H to 0003ECH	—	—	—	—	Reserved
0003F0H	BSD0 (W) W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Bit Search Module
0003F4H	BSD1 (R/W) W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0003F8H	BSDC (W) W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0003FCH	BSRR (R) W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000400H	DDR0 (R/W) B, H, W 00000000	DDR1 (R/W) B, H, W 00000000	DDR2 (R/W) B, H, W 00000000	DDR3 (R/W) B, H, W 00000000	Data Direction Register
000404H	DDR4 (R/W) B, H, W 00000000	DDR5 (R/W) B, H, W 00000000	DDR6 (R/W) B, H, W ---00000	DDR7 (R/W) B, H, W 00000000	
000408H	DDR8 (R/W) B, H, W --000000	DDR9 (R/W) B, H, W 00000000	DDRA (R/W) B, H, W 00000000	DDRB (R/W) B, H, W 00000000	
00040CH	DDRC (R/W) B, H, W 00000000	DDRD (R/W) B, H, W 00000000	DDRE (R/W) B, H, W -----000	DDRF (R/W) B, H, W 00000000	
000410H to 00041CH	—	—	—	—	Reserved
000420H	PFR0 (R/W) B, H, W 0000-00-	PFR1 (R/W) B, H, W 00-00-0-	PFR2 (R/W) B, H, W 00000000	PFR3 (R/W) B, H, W ------00	Port Function Register
000424H	PFR4 (R/W) B, H, W 00000000	PFR5 (R/W) B, H, W -0000000	PFR6 (R/W) B, H, W ------00	PFR7 (R/W) B, H, W 00000-0-	
000428H	PFR8 (R/W) B, H, W 000-----	PFR9 (R/W) B, H, W 00000000	PFRA (R/W) B, H, W -----000	PFRB (R/W) B, H, W --------	
00042CH	PFRC (R/W) B, H, W --------	PFRD (R/W) B, H, W 00-00-0-	PFRE (R/W) B, H, W -----00-	PFRF (R/W) B, H, W --------	

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
000430H to 00043CH	—	—	—	—	Reserved
000440H	ICR00 (R, R/W) B, H, W ---11111	ICR01 (R, R/W) B, H, W ---11111	ICR02 (R, R/W) B, H, W ---11111	ICR03 (R, R/W) B, H, W ---11111	Interrupt Control Unit
000444H	ICR04 (R, R/W) B, H, W ---11111	ICR05 (R, R/W) B, H, W ---11111	ICR06 (R, R/W) B, H, W ---11111	ICR07 (R, R/W) B, H, W ---11111	
000448H	ICR08 (R, R/W) B, H, W ---11111	ICR09 (R, R/W) B, H, W ---11111	ICR10 (R, R/W) B, H, W ---11111	ICR11 (R, R/W) B, H, W ---11111	
00044CH	ICR12 (R, R/W) B, H, W ---11111	ICR13 (R, R/W) B, H, W ---11111	ICR14 (R, R/W) B, H, W ---11111	ICR15 (R, R/W) B, H, W ---11111	
000450H	ICR16 (R, R/W) B, H, W ---11111	ICR17 (R, R/W) B, H, W ---11111	ICR18 (R, R/W) B, H, W ---11111	ICR19 (R, R/W) B, H, W ---11111	
000454H	ICR20 (R, R/W) B, H, W ---11111	ICR21 (R, R/W) B, H, W ---11111	ICR22 (R, R/W) B, H, W ---11111	ICR23 (R, R/W) B, H, W ---11111	
000458H	ICR24 (R, R/W) B, H, W ---11111	ICR25 (R, R/W) B, H, W ---11111	ICR26 (R, R/W) B, H, W ---11111	ICR27 (R, R/W) B, H, W ---11111	
00045CH	ICR28 (R, R/W) B, H, W ---11111	ICR29 (R, R/W) B, H, W ---11111	ICR30 (R, R/W) B, H, W ---11111	ICR31 (R, R/W) B, H, W ---11111	
000460H	ICR32 (R, R/W) B, H, W ---11111	ICR33 (R, R/W) B, H, W ---11111	ICR34 (R, R/W) B, H, W ---11111	ICR35 (R, R/W) B, H, W ---11111	
000464H	ICR36 (R, R/W) B, H, W ---11111	ICR37 (R, R/W) B, H, W ---11111	ICR38 (R, R/W) B, H, W ---11111	ICR39 (R, R/W) B, H, W ---11111	
000468H	ICR40 (R, R/W) B, H, W ---11111	ICR41 (R, R/W) B, H, W ---11111	ICR42 (R, R/W) B, H, W ---11111	ICR43 (R, R/W) B, H, W ---11111	
00046CH	ICR44 (R, R/W) B, H, W ---11111	ICR45 (R, R/W) B, H, W ---11111	ICR46 (R, R/W) B, H, W ---11111	ICR47 (R, R/W) B, H, W ---11111	
000470H to 00047CH	—	—	—	—	Reserved

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
000480H	RSRR (R, R/W) B, H, W X-***-00*2	STCR (R/W) B, H, W 00110011	TBCR (R/W, R) B, H, W 00XXXX11	CTBR (W) B, H, W XXXXXXXX	Clock Control Unit
000484H	CLKR (R/W) B, H, W 00000000	WPR (W) B, H, W XXXXXXXX	DIVR0 (R/W) B, H, W 00000011	DIVR1 (R/W) B, H, W 00000000	
000488H	—	—	OSCCR (R/W) B XXXXXXX0	—	
00048CH	—	—	—	—	Reserved
000490H	OSCR (R/W, W) B 000XX000	—	—	—	Main Stabilization Wait Timer
000494H	PLLC (R/W, R) B, H, W X1000101	—	—	—	PLL Controller
000498H to 0004FCH	—	—	—	—	Reserved
000500H	PPER0 (R/W) B, H, W 00000000	PPER1 (R/W) B, H, W 00000000	PPER2 (R/W) B, H, W 00000000	PPER3 (R/W) B, H, W 00000000	Port Pull-up/ Pull-down Enable Register
000504H	PPER4 (R/W) B, H, W 00000000	PPER5 (R/W) B, H, W 00000000	PPER6 (R/W) B, H, W ---00000	PPER7 (R/W) B, H, W 00000000	
000508H	PPER8 (R/W) B, H, W --000000	PPER9 (R/W) B, H, W 00000000	PPERA (R/W) B, H, W 00000000	PPERB (R/W) B, H, W 00000000	
00050CH	PPERC (R/W) B, H, W 00000000	PPERD (R/W) B, H, W 00000000	PPERE (R/W) B, H, W -----000	PPERF (R/W) B, H, W 00000000	
000510H to 00051CH	—	—	—	—	Reserved

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
000520H	PPCR0 (R/W) B, H, W 11111111	PPCR1 (R/W) B, H, W 11111111	PPCR2 (R/W) B, H, W 11111111	PPCR3 (R/W) B, H, W 11111111	Port Pull-up/ Pull-down Control Register
000524H	PPCR4 (R/W) B, H, W 11111111	PPCR5 (R/W) B, H, W 11111111	PPCR6 (R/W) B, H, W ---11111	PPCR7 (R/W) B, H, W 11111111	
000528H	PPCR8 (R/W) B, H, W --111111	PPCR9 (R/W) B, H, W 11111111	PPCRA (R/W) B, H, W 11111111	PPCRB (R/W) B, H, W 11111111	
00052CH	PPCRC (R/W) B, H, W 11111111	PPCRD (R/W) B, H, W 11111111	PPCRE (R/W) B, H, W -----111	PPCRF (R/W) B, H, W 11111111	
000530H to 00053CH	—	—	—	—	Reserved
000540H	PILR0 (R/W) B, H, W 00000000	PILR1 (R/W) B, H, W 00000000	PILR2 (R/W) B, H, W 00000000	PILR3 (R/W) B, H, W 00000000	Port Input Level Select Register
000544H	PILR4 (R/W) B, H, W 00000000	PILR5 (R/W) B, H, W 00000000	PILR6 (R/W) B, H, W ---00000	PILR7 (R/W) B, H, W 00000000	
000548H	PILR8 (R/W) B, H, W --000000	PILR9 (R/W) B, H, W 00000000	PILRA (R/W) B, H, W 00000000	PILRB (R/W) B, H, W 00000000	
00054CH	PILRC (R/W) B, H, W 00000000	PILRD (R/W) B, H, W 00000000	PILRE (R/W) B, H, W -----000	PILRF (R/W) B, H, W 00000000	
000550H to 00061CH	—	—	—	—	Reserved
000620H	PIDR0 (R) B, H, W XXXXXXXX	PIDR1 (R) B, H, W XXXXXXXX	PIDR2 (R) B, H, W XXXXXXXX	PIDR3 (R) B, H, W XXXXXXXX	Input Data Direct Read Register
000624H	PIDR4 (R) B, H, W XXXXXXXX	PIDR5 (R) B, H, W XXXXXXXX	PIDR6 (R) B, H, W ---XXXXX	PIDR7 (R) B, H, W XXXXXXXX	
000628H	PIDR8 (R) B, H, W --XXXXXX	PIDR9 (R) B, H, W XXXXXXXX	PIDRA (R) B, H, W XXXXXXXX	PIDRB (R) B, H, W XXXXXXXX	
00062CH	PIDRC (R) B, H, W XXXXXXXX	PIDRD (R) B, H, W XXXXXXXX	PIDRE (R) B, H, W -----XXX	PIDRF (R) B, H, W XXXXXXXX	
000630H to 000FFCH	—	—	—	—	Reserved

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
001000H	DMASA0 (R/W) W 00000000 00000000 00000000 00000000				DMA Controller
001004H	DMADA0 (R/W) W 00000000 00000000 00000000 00000000				
001008H	DMASA1 (R/W) W 00000000 00000000 00000000 00000000				
00100CH	DMADA1 (R/W) W 00000000 00000000 00000000 00000000				
001010H	DMASA2 (R/W) W 00000000 00000000 00000000 00000000				
001014H	DMADA2 (R/W) W 00000000 00000000 00000000 00000000				
001018H	DMASA3 (R/W) W 00000000 00000000 00000000 00000000				
00101CH	DMADA3 (R/W) W 00000000 00000000 00000000 00000000				
001020H	DMASA4 (R/W) W 00000000 00000000 00000000 00000000				
001024H	DMADA4 (R/W) W 00000000 00000000 00000000 00000000				
001028H to 006FFCH	—	—	—	—	Reserved
007000H	FLCR (R/W, R) B, H, W 0000X101	—	—	—	Flash Interface
007004H	FLWC (R/W) B, H, W 01011011	—	—	—	
007008H to 01FFFCH	—	—	—	—	Reserved

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
020000H	CTRLR0 (R/W, R) B, H, W 00000000 00000001		STATR0 (R/W, R) B, H, W 00000000 00000000		CAN Controller 0
020004H	ERRCNT0 (R) B, H, W 00000000 00000000		BTR0 (R/W, R) B, H, W 00100011 00000001		
020008H	INTR0 (R) B, H, W 00000000 00000000		TESTR0 (R/W, R) B, H, W 00000000 r0000000*3		
02000CH	BRPER0 (R, R/W) B, H, W 00000000 00000000		—	—	
020010H	IF1CREQ0 (R/W, R) B, H, W 00000000 00000001		IF1CMSK0 (R/W, R) B, H, W 00000000 00000000		
020014H	IF1MSK20 (R/W, R) B, H, W 11111111 11111111		IF1MSK10 (R/W) B, H, W 11111111 11111111		
020018H	IF1ARB20 (R/W) B, H, W 00000000 00000000		IF1ARB10 (R/W) B, H, W 00000000 00000000		
02001CH	IF1MCTR0 (R/W, R) B, H, W 00000000 00000000		—	—	
020020H	IF1DTA10 (R/W) B, H, W 00000000 00000000		IF1DTA20 (R/W) B, H, W 00000000 00000000		
020024H	IF1DTB10 (R/W) B, H, W 00000000 00000000		IF1DTB20 (R/W) B, H, W 00000000 00000000		
020028H to 02002CH	—	—	—	—	Reserved
020030H	IF1DTA20 (R/W) B, H, W 00000000 00000000		IF1DTA10 (R/W) B, H, W 00000000 00000000		CAN Controller 0
020034H	IF1DTB10 (R/W) B, H, W 00000000 00000000		IF1DTB20 (R/W) B, H, W 00000000 00000000		
020038H to 02003CH	—	—	—	—	Reserved

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
020040H	IF2CREQ0 (R/W, R) B, H, W 00000000 00000001		IF2CMSK0 (R/W, R) B, H, W 00000000 00000000		CAN Controller 0
020044H	IF2MSK20 (R/W, R) B, H, W 11111111 11111111		IF2MSK10 (R/W) B, H, W 11111111 11111111		
020048H	IF2ARB20 (R/W) B, H, W 00000000 00000000		IF2ARB10 (R/W) B, H, W 00000000 00000000		
02004CH	IF2MCTR0 (R/W, R) B, H, W 00000000 00000000		—	—	
020050H	IF2DTA10 (R/W) B, H, W 00000000 00000000		IF2DTA20 (R/W) B, H, W 00000000 00000000		
020054H	IF2DTB10 (R/W) B, H, W 00000000 00000000		IF2DTB20 (R/W) B, H, W 00000000 00000000		
020058H, 02005CH	—	—	—	—	Reserved
020060H	IF2DTA20 (R/W) B, H, W 00000000 00000000		IF2DTA10 (R/W) B, H, W 00000000 00000000		CAN Controller 0
020064H	IF2DTB20 (R/W) B, H, W 00000000 00000000		IF2DTB10 (R/W) B, H, W 00000000 00000000		
020068H to 02007CH	—	—	—	—	Reserved
020080H	TREQR20 (R) B, H, W 00000000 00000000		TREQR10 (R) B, H, W 00000000 00000000		CAN Controller 0
020084H to 02008CH	—	—	—	—	Reserved
020090H	NEWDT20 (R) B, H, W 00000000 00000000		NEWDT10 (R) B, H, W 00000000 00000000		CAN Controller 0
020094H to 02009CH	—	—	—	—	Reserved
0200A0H	INTPND20 (R) B, H, W 00000000 00000000		INTPND10 (R) B, H, W 00000000 00000000		CAN Controller 0

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
0200A4H to 0200ACH	—	—	—	—	Reserved
0200B0H	MSGVAL20 (R) B, H, W 00000000 00000000		MSGVAL10 (R) B, H, W 00000000 00000000		CAN Controller 0
0200B4H to 0200FCH	—	—	—	—	Reserved
020100H	CTRLR1 (R/W, R) B, H, W 00000000 00000001		STATR1 (R/W, R) B, H, W 00000000 00000000		CAN Controller 1
020104H	ERRCNT1 (R) B, H, W 00000000 00000000		BTR1 (R/W, R) B, H, W 00100011 00000001		
020108H	INTR1 (R) B, H, W 00000000 00000000		TESTR1 (R/W, R) B, H, W 00000000 r0000000*3		
02010CH	BRPER1 (R, R/W) B, H, W 00000000 00000000		—	—	
020110H	IF1CREQ1 (R/W, R) B, H, W 00000000 00000001		IF1CMSK1 (R/W, R) B, H, W 00000000 00000000		
020114H	IF1MSK21 (R/W, R) B, H, W 11111111 11111111		IF1MSK11 (R/W) B, H, W 11111111 11111111		
020118H	IF1ARB21 (R/W) B, H, W 00000000 00000000		IF1ARB11 (R/W) B, H, W 00000000 00000000		
02011CH	IF1MCTR1 (R/W, R) B, H, W 00000000 00000000		—	—	
020120H	IF1DTA11 (R/W) B, H, W 00000000 00000000		IF1DTA21 (R/W) B, H, W 00000000 00000000		
020124H	IF1DTB11 (R/W) B, H, W 00000000 00000000		IF1DTB21 (R/W) B, H, W 00000000 00000000		
020128H, 02012CH	—	—	—	—	Reserved

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
020130H	IF1DTA21 (R/W) B, H, W 00000000 00000000		IF1DTA11 (R/W) B, H, W 00000000 00000000		CAN Controller 1
020134H	IF1DTB11 (R/W) B, H, W 00000000 00000000		IF1DTB21 (R/W) B, H, W 00000000 00000000		
020138H, 02013CH	—	—	—	—	Reserved
020140H	IF2CREQ1 (R/W, R) B, H, W 00000000 00000001		IF2CMSK1 (R/W, R) B, H, W 00000000 00000000		CAN Controller 1
020144H	IF2MSK21 (R/W, R) B, H, W 11111111 11111111		IF2MSK11 (R/W) B, H, W 11111111 11111111		
020148H	IF2ARB21 (R/W) B, H, W 00000000 00000000		IF2ARB11 (R/W) B, H, W 00000000 00000000		
02014CH	IF2MCTR1 (R/W, R) B, H, W 00000000 00000000		—	—	
020150H	IF2DTA11 (R/W) B, H, W 00000000 00000000		IF2DTA21 (R/W) B, H, W 00000000 00000000		
020154H	IF2DTB11 (R/W) B, H, W 00000000 00000000		IF2DTB21 (R/W) B, H, W 00000000 00000000		
020158H, 02015CH	—	—	—	—	Reserved
020160H	IF2DTA21 (R/W) B, H, W 00000000 00000000		IF2DTA11 (R/W) B, H, W 00000000 00000000		CAN Controller 1
020164H	IF2DTB21 (R/W) B, H, W 00000000 00000000		IF2DTB11 (R/W) B, H, W 00000000 00000000		
020168H to 02017CH	—	—	—	—	Reserved

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
020180H	TREQR21 (R) B, H, W 00000000 00000000		TREQR11 (R) B, H, W 00000000 00000000		CAN Controller 1
020184H to 02018CH	—	—	—	—	Reserved
020190H	NEWDT21 (R) B, H, W 00000000 00000000		NEWDT11 (R) B, H, W 00000000 00000000		CAN Controller 1
020194H to 02019CH	—	—	—	—	Reserved
0201A0H	INTPND21 (R) B, H, W 00000000 00000000		INTPND11 (R) B, H, W 00000000 00000000		CAN Controller 1
0201A4H to 0201ACH	—	—	—	—	Reserved
0201B0H	MSGVAL21 (R) B, H, W 00000000 00000000		MSGVAL11 (R) B, H, W 00000000 00000000		CAN Controller 1
0200B4H to 0200FCH	—	—	—	—	Reserved
020200H	CTRLR2 (R/W, R) B, H, W 00000000 00000001		STATR2 (R/W, R) B, H, W 00000000 00000000		CAN Controller 2
020204H	ERRCNT2 (R) B, H, W 00000000 00000000		BTR2 (R/W, R) B, H, W 00100011 00000001		
020208H	INTR2 (R) B, H, W 00000000 00000000		TESTR2 (R/W, R) B, H, W 00000000 r0000000*3		
02020CH	BRPER2 (R, R/W) B, H, W 00000000 00000000		—	—	
020210H	IF1CREQ2 (R/W, R) B, H, W 00000000 00000001		IF1CMSK2 (R/W, R) B, H, W 00000000 00000000		
020214H	IF1MSK22 (R/W, R) B, H, W 11111111 11111111		IF1MSK12 (R/W) B, H, W 11111111 11111111		

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
020218H	IF1ARB22 (R/W) B, H, W 00000000 00000000		IF1ARB12 (R/W) B, H, W 00000000 00000000		CAN Controller 2
02021CH	IF1MCTR2 (R/W, R) B, H, W 00000000 00000000		—	—	
020220H	IF1DTA12 (R/W) B, H, W 00000000 00000000		IF1DTA22 (R/W) B, H, W 00000000 00000000		
020224H	IF1DTB12 (R/W) B, H, W 00000000 00000000		IF1DTB22 (R/W) B, H, W 00000000 00000000		
020228H, 02022CH	—	—	—	—	Reserved
020230H	IF1DTA22 (R/W) B, H, W 00000000 00000000		IF1DTA12 (R/W) B, H, W 00000000 00000000		CAN Controller 2
020234H	IF1DTB22 (R/W) B, H, W 00000000 00000000		IF1DTB12 (R/W) B, H, W 00000000 00000000		
020238H, 02023CH	—	—	—	—	Reserved
020240H	IF2CREQ2 (R/W, R) B, H, W 00000000 00000001		IF2CMSK2 (R/W, R) B, H, W 00000000 00000000		CAN Controller 2
020244H	IF2MSK22 (R/W, R) B, H, W 11111111 11111111		IF2MSK12 (R/W) B, H, W 11111111 11111111		
020248H	IF2ARB22 (R/W) B, H, W 00000000 00000000		IF2ARB12 (R/W) B, H, W 00000000 00000000		
02024CH	IF2MCTR2 (R/W, R) B, H, W 00000000 00000000		—	—	
020250H	IF2DTA12 (R/W) B, H, W 00000000 00000000		IF2DTA22 (R/W) B, H, W 00000000 00000000		
020254H	IF2DTB12 (R/W) B, H, W 00000000 00000000		IF2DTB22 (R/W) B, H, W 00000000 00000000		

(Continued)

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
020258H, 02025CH	—	—	—	—	Reserved
020260H	IF2DTA22 (R/W) B, H, W 00000000 00000000		IF2DTA12 (R/W) B, H, W 00000000 00000000		CAN Controller 2
020264H	IF2DTB22 (R/W) B, H, W 00000000 00000000		IF2DTB12 (R/W) B, H, W 00000000 00000000		
020268H to 02027CH	—	—	—	—	Reserved
020280H	TREQR22 (R) B, H, W 00000000 00000000		TREQR12 (R) B, H, W 00000000 00000000		CAN Controller 2
020284H to 02028CH	—	—	—	—	Reserved
020290H	NEWDT22 (R) B, H, W 00000000 00000000		NEWDT12 (R) B, H, W 00000000 00000000		CAN Controller 2
020294H to 02029CH	—	—	—	—	Reserved
0202A0H	INTPND22 (R) B, H, W 00000000 00000000		INTPND12 (R) B, H, W 00000000 00000000		CAN Controller 2
0202A4H to 0202ACH	—	—	—	—	Reserved
0202B0H	MSGVAL22 (R) B, H, W 00000000 00000000		MSGVAL12 (R) B, H, W 00000000 00000000		CAN Controller 2

*1 : The lower 16 bits (DTC[15:0]) cannot be accessed in bytes.

*2 : It differs depending on the source.

*3 : As for bit7, the level of the RX pin is read.

■ INTERRUPT VECTOR

Interrupt source	Interrupt number		Interrupt level	Offset	TBR default address
	Decimal	Hexa-decimal			
Reset*	0	00	—	$3FC_H$	$000FFFFC_H$
Mode vector*	1	01	—	$3F8_H$	$000FFFF8_H$
System reserved	2	02	—	$3F4_H$	$000FFFF4_H$
System reserved	3	03	—	$3F0_H$	$000FFFF0_H$
System reserved	4	04	—	$3EC_H$	$000FFFEC_H$
System reserved	5	05	—	$3E8_H$	$000FFFE8_H$
System reserved	6	06	—	$3E4_H$	$000FFFE4_H$
Coprocessor absent trap	7	07	—	$3E0_H$	$000FFFE0_H$
Coprocessor error trap	8	08	—	$3DC_H$	$000FFFDC_H$
INTE instruction	9	09	—	$3D8_H$	$000FFFD8_H$
System reserved	10	0A	—	$3D4_H$	$000FFFD4_H$
System reserved	11	0B	—	$3D0_H$	$000FFFD0_H$
Step trace trap	12	0C	—	$3CC_H$	$000FFFCC_H$
NMI request (ICE)	13	0D	—	$3C8_H$	$000FFFC8_H$
Undefined instruction exception	14	0E	—	$3C4_H$	$000FFFC4_H$
NMI request	15	0F	15 (F_H) Fixed	$3C0_H$	$000FFFC0_H$
External interrupt 0	16	10	ICR00	$3BC_H$	$000FFFBC_H$
External interrupt 1	17	11	ICR01	$3B8_H$	$000FFFB8_H$
External interrupt 2	18	12	ICR02	$3B4_H$	$000FFFB4_H$
External interrupt 3	19	13	ICR03	$3B0_H$	$000FFFB0_H$
External interrupt 4	20	14	ICR04	$3AC_H$	$000FFFAC_H$
External interrupt 5	21	15	ICR05	$3A8_H$	$000FFFA8_H$
External interrupt 6	22	16	ICR06	$3A4_H$	$000FFFA4_H$
External interrupt 7	23	17	ICR07	$3A0_H$	$000FFFA0_H$
Reload timer 0	24	18	ICR08	$39C_H$	$000FFF9C_H$
Reload timer 1	25	19	ICR09	398_H	$000FFF98_H$
Reload timer 2	26	1A	ICR10	394_H	$000FFF94_H$
UART 0 (Reception)	27	1B	ICR11	390_H	$000FFF90_H$
UART 0 (Transmission)	28	1C	ICR12	$38C_H$	$000FFF8C_H$
UART 1 (Reception)	29	1D	ICR13	388_H	$000FFF88_H$
UART 1 (Transmission)	30	1E	ICR14	384_H	$000FFF84_H$
UART 2 (Reception)	31	1F	ICR15	380_H	$000FFF80_H$
UART 2 (Transmission)	32	20	ICR16	$37C_H$	$000FFF7C_H$

(Continued)

Interrupt source	Interrupt number		Interrupt level	Offset	TBR default address
	Decimal	Hexa-decimal			
CAN 0	33	21	ICR17	378H	000FFF78H
CAN 1	34	22	ICR18	374H	000FFF74H
UART 3/5 (Reception)	35	23	ICR19	370H	000FFF70H
UART 3/5 (Transmission)	36	24	ICR20	36CH	000FFF6CH
UART 4/6 (Reception)	37	25	ICR21	368H	000FFF68H
UART 4/6 (Transmission)	38	26	ICR22	364H	000FFF64H
A/D converter	39	27	ICR23	360H	000FFF60H
RTC/CAN 2	40	28	ICR24	35CH	000FFF5CH
ICU 0	41	29	ICR25	358H	000FFF58H
ICU 1	42	2A	ICR26	354H	000FFF54H
ICU 2/3	43	2B	ICR27	350H	000FFF50H
ICU 4/5/6/7	44	2C	ICR28	34CH	000FFF4CH
FRT 0/1/2/3	45	2D	ICR29	348H	000FFF48H
Main oscillation stabilization wait timer	46	2E	ICR30	344H	000FFF44H
Time-base timer overflow	47	2F	ICR31	340H	000FFF40H
OUT 0/1/2/3	48	30	ICR32	33CH	000FFF3CH
OUT 4/5/6/7	49	31	ICR33	338H	000FFF38H
PPG 0	50	32	ICR34	334H	000FFF34H
PPG 1	51	33	ICR35	330H	000FFF30H
PPG 2/3	52	34	ICR36	32CH	000FFF2CH
PPG 4/5/6/7	53	35	ICR37	328H	000FFF28H
PPG 8/9/A/B	54	36	ICR38	324H	000FFF24H
PPG C/D/E/F	55	37	ICR39	320H	000FFF20H
External interrupt 8	56	38	ICR40	31CH	000FFF1CH
External interrupt 9	57	39	ICR41	318H	000FFF18H
External interrupt 10	58	3A	ICR42	314H	000FFF14H
External interrupt 11	59	3B	ICR43	310H	000FFF10H
External interrupt 12/13	60	3C	ICR44	30CH	000FFF0CH
External interrupt 14/15	61	3D	ICR45	308H	000FFF08H
DMA (End, Error)	62	3E	ICR46	304H	000FFF04H
Delay interrupt source bit	63	3F	ICR47	300H	000FFF00H
System reserved (Used by REALOS)	64	40	—	2FCH	000FFEFCH

(Continued)

(Continued)

Interrupt source	Interrupt number		Interrupt level	Offset	TBR default address
	Decimal	Hexa-decimal			
System reserved (Used by REALOS)	65	41	—	2F8H	000FFEF8H
System reserved	66	42	—	2F4H	000FFEF4H
System reserved	67	43	—	2F0H	000FFEF0H
System reserved	68	44	—	2ECH	000FFEECH
System reserved	69	45	—	2E8H	000FFEE8H
System reserved	70	46	—	2E4H	000FFEE4H
System reserved	71	47	—	2E0H	000FFEE0H
System reserved	72	48	—	2DCH	000FFEDCH
System reserved	73	49	—	2D8H	000FFED8H
System reserved	74	4A	—	2D4H	000FFED4H
System reserved	75	4B	—	2D0H	000FFED0H
System reserved	76	4C	—	2CCH	000FFECCH
System reserved	77	4D	—	2C8H	000FFEC8H
System reserved	78	4E	—	2C4H	000FFEC4H
System reserved	79	4F	—	2C0H	000FFEC0H
Used in INT instruction	80 to 255	50 to FF	—	2BCH to 000H	000FFEBCH to 000FFC00H

* : Even though the TBR value is changed, fixed addresses, 000FFFFCH and 000FFFF8H, are always used for the reset vector and the mode vector.

■ PIN STATUS IN EACH CPU STATE

Terms used as the status of pins mean as follows.

- Input enabled
  Indicates that the input function can be used.
- Output Hi-Z
  Means the placing of a pin in a high impedance state by preventing the transistor for driving the pin from driving.
- Output maintained
  Indicates the output in the output state existing immediately before this mode is established. If the device enters this mode with an internal output peripheral operating or while serving as an output port, the output is performed by the internal peripheral or the port output is maintained, respectively.
- State existing immediately before is maintained.
  When the device serves for output or input immediately before entering this mode, the device maintains the output or is ready for the input, respectively.
- Pull-down
  Built-in pull-down resistor is valid.

Table of Pin Status in Each Mode

- Single chip mode

Pin name	Function name	Initial value		In sleep state	In stop state	
		INITX = "L"	**INITX = "H"**		**HIZ = 0**	**HIZ = 1**
INITX	INITX	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
X0	X0				Pull-down	Pull-down
X1	X1					
X0A	X0A					
X1A	X1A					
MD0	MD0				Input enabled	Input enabled
MD1	MD1					
MD2	MD2					
MD3	MD3					
P00	P00/SIN5/INT8R	Output Hi-Z input enabled	Output Hi-Z input enabled	P : Immediately preceding status held F : Normal operation performed	P : Immediately preceding status held F : Output held or Hi-Z , input enabled	Output Hi-Z/ selecting interrupt function, and input enabled when interrupt is allowed during ENIR internal input held
P01	P01/SOT5/INT9R					
P02	P02/SCK5/INT10R					
P03	P03/SIN6/INT11R					
P04	P04/SOT6/INT12R					
P05	P05/SCK6/INT13R					
P06	P06/OUT4/INT14R					
P07	P07/OUT5/INT15R					
P10	P10/TIN1					Output Hi-Z internal input held
P11	P11/TOT1					
P12	P12/SIN3					
P13	P13/SOT3					
P14	P14/SCK3					
P15	P15/SIN4					
P16	P16/SOT4					
P17	P17/SCK4					
P20 to P27	P20 to P27/ PPG0, 2, 4, 6, 8, A, C, E					

(Continued)

Pin name	Function name	Initial value		In sleep state	In stop state	
		INITX = "L"	INITX = "H"		HIZ = 0	HIZ = 1
P30	P30/ (RX2) / (INT10C)	Output Hi-Z input enabled	Output Hi-Z input enabled	P : Immediately preceding status held F : Normal operation performed	P : Immediately preceding status held F : Output held or Hi-Z , input enabled	Output Hi-Z/ selecting interrupt function, and input enabled when interrupt is allowed during ENIR internal input held
P31	P31/ (TX2)					Output Hi-Z internal input held
P32	P32/INT10					Output Hi-Z/ selecting interrupt function, and input enabled when interrupt is allowed during ENIR internal input held
P33 to P37	P33 to P37/ INT11 to INT15					
P40 to P43	P40 to P43/ PPG9, B, D, F					Output Hi-Z internal input held
P44 to P47	P44 to P47/ IN0 to IN3					
P50 to P53	P50 to P53/ PPG1, 3, 5, 7					
P54	P54/IN4					
P55	P55/IN5					
P56	P56/IN6					
P57	P57/IN7					
P60	P60/OUT6					
P61	P61/OUT7					
P62	P62					
P63	P63					
P64	P64					
P70	P70/RX0/INT8					Output Hi-Z/ selecting interrupt function, and input enabled when interrupt is allowed during ENIR internal input held
P71	P71/TX0					Output Hi-Z internal input held

(Continued)

Pin name	Function name	Initial value		In sleep state	In stop state	
		INITX = "L"	INITX = "H"		HIZ = 0	HIZ = 1
P72	P72/RX1/INT9	Output Hi-Z input enabled	Output Hi-Z input enabled	P : Immediately preceding status held F : Normal operation performed	P : Immediately preceding status held F : Output held or Hi-Z , input enabled	Output Hi-Z/ selecting interrupt function, and input enabled when interrupt is allowed during ENIR internal input held
P73	P73/TX1					Output Hi-Z internal input held
P74 to P77	P74 to P77/ OUT0 to OUT3					
P80 to P83	P80 to P83/ FRCK0 to FRCK3					
P84	P84/TIN2					
P85	P85/TOT2					
P90 to P97	P90 to P97/PPG0R, 2R, 4R, 6R, 8R, AR, CR, ER/AN0 to AN7					Output Hi-Z internal input held
PA0	PA0/SIN2R/AN8					
PA1	PA1/SOT2R/AN9					
PA2	PA2/SCK2R/AN10					
PA3 to PA7	PA3 to PA7/ AN11 to AN15					
PB0 to PB7	PB0 to PB7/ INT0R to INT7R/ AN16 to AN23					Output Hi-Z/ selecting interrupt function, and input enabled when interrupt is allowed during ENIR internal input held
PC0 to PC7	PC0 to PC7/ AN24 to AN31					Output Hi-Z internal input held

(Continued)

(Continued)

Pin name	Function name	Initial value		In sleep state	In stop state	
		INITX = "L"	INITX = "H"		HIZ = 0	HIZ = 1
PD0	PD0/TIN0/ATGX	Output Hi-Z input enabled	Output Hi-Z input enabled	P : Immediately preceding status held F : Normal operation performed	P : Immediately preceding status held F : Output held or Hi-Z , input enabled	Output Hi-Z internal input held
PD1	PD1/TOT0					
PD2	PD2/SIN0					
PD3	PD3/SOT0					
PD4	PD4/SCK0					
PD5	PD5/SIN1					
PD6	PD6/SOT1					
PD7	PD7/SCK1					
PE0	PE0/SIN2					
PE1	PE1/SOT2					
PE2	PE2/SCK2					
PF0 to PF7	PF0 to PF7/ INT0 to INT7					Output Hi-Z/ selecting interrupt function, and input enabled when interrupt is allowed during ENIR internal input held

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage	V_{CC}	V_{SS} – 0.3	V_{SS} + 6.0	V	
	AV_{CC}	V_{SS} – 0.3	V_{SS} + 6.0	V	$AV_{CC} = V_{CC}$*1
	AVRH	V_{SS} – 0.3	V_{SS} + 6.0	V	$AV_{CC} \geq$ AVRH
Input voltage	V_I	V_{SS} – 0.3	V_{CC} + 0.3	V	
Output voltage	V_O	V_{SS} – 0.3	V_{CC} + 0.3	V	
Maximum clamp current	I_{CLAMP}	– 2.0	+ 2.0	mA	*5
Total maximum clamp current	ΣI_{CLAMP}	—	20	mA	*5
“L” level maximum output current*2	I_{OL1}	—	8	mA	
“L” level average output current*3	I_{OLAV1}	—	2	mA	
“L” level total maximum output current	ΣI_{OL1}	—	64	mA	
“L” level total average output current*4	ΣI_{OLAV1}	—	25	mA	
“H” level maximum output current*2	I_{OH1}	—	– 8	mA	
“H” level average output current*3	I_{OHAV1}	—	– 2	mA	
“H” level total maximum output current	ΣI_{OH1}	—	– 64	mA	
“H” level total average output current*4	ΣI_{OHAV1}	—	– 25	mA	
Power consumption	P_D	—	500	mW	
Operating temperature	Ta	– 40	+ 105	°C	Single-chip mode
Storage temperature	T_{stg}	– 55	+ 150	°C	

*1: Caution must be taken that AV_{CC} does not exceed V_{CC} upon power-on and under other circumstances.

*2: The maximum output current defines the peak current value of each of the corresponding pins.

*3: The average output current defines the average value of the current (100 ms) which passes through each of the corresponding pins. The average value represents a value calculated by multiplying the operating current by the operating rate.

*4: The total average output current defines the average value of the current (100 ms) which passes through all the corresponding pins. The average value represents a value calculated by multiplying the operating current by the operating rate.

*5:
- Corresponding pins : P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P64, P70 to P77, P80 to P85, P90 to P97, PA0 to PA7, PB0 to PB7, PC0 to PC7, PD0 to PD7, PE0 to PE2,PF0 to PF7
- Use within recommended operating conditions.
- Use at DC voltage (current).
- The + B signal should always be applied a limiting resistor placed between the + B signal and the microcontroller.
- The value of the limiting resistor should be set so that when the + B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
- Note that, when the microcontroller drive current is low as in low power consumption mode, the + B input potential can increase the potential at the VCC pin via a protection diode, possibly affecting other devices.

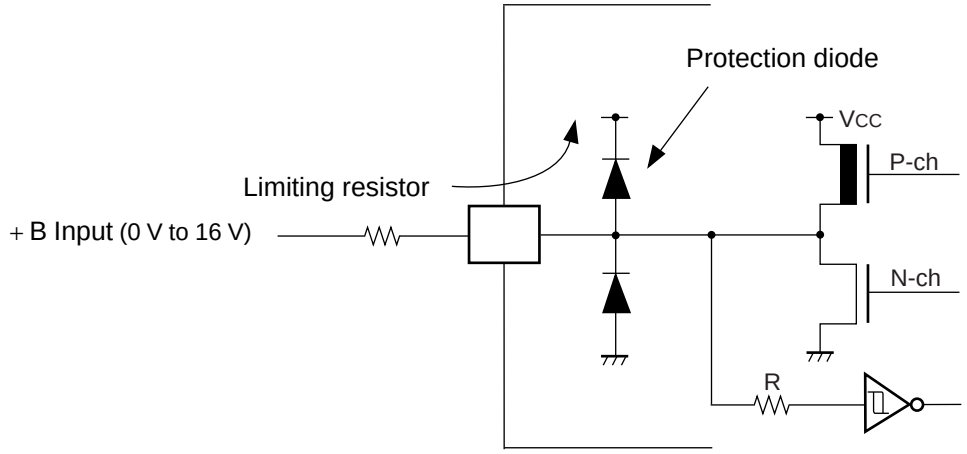
(Continued)

(Continued)

- Note that, if the + B input exists when the microcontroller is off (not fixed at 0 V), power is supplied through the pin, possibly causing the microcontroller to operate imperfectly.
  Note that, if the + B input exists when the power supply is turned on, power is supplied through the pin, possibly resulting in a power-supply voltage at which a power-on reset does not work.
- Be careful not to let the + B input pin open.
- Note that the analog I/O pins (such as the LCD drive and comparator input pins) other than the A/D input pin cannot input + B.

- **Recommended example circuit**

• Input/output equivalent circuits



WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

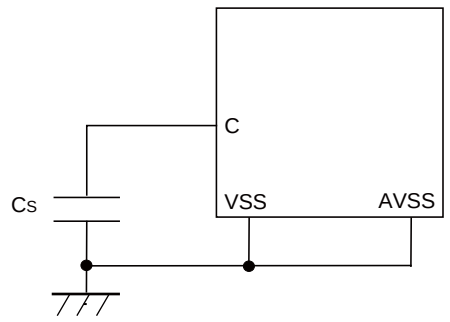
2. Recommended operation condition

(V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Power supply voltage	V_{CC} AV_{CC}	3.5	5.5	V	Normal operation
	V_{CC}	3.0	5.5	V	RAM data retention at STOP operation
Smoothing capacitor*	C_S	1 (within tolerance ± 50%)		µF	Use a ceramic capacitor or a capacitor with similar frequency characteristics. Use a bypass capacitor for the VCC pin, which has larger than C_S.
Operating temperature	Ta	− 40	+ 105	°C	Single-chip mode

* : For how to connect the smoothing capacitor C_S, see the figure below.

• C Pin Connection Diagram



WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

3. DC Specifications

(Ta: Recommended operating conditions; V_{CC} = 5.0 V ±10%, V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage	V_{IHS}	—	—	$0.8 \times V_{CC}$	—	$V_{CC} + 0.3$	V	CMOS automotive input
	V_{IHC}	—	—	$0.7 \times V_{CC}$	—	$V_{CC} + 0.3$	V	CMOS Schmitt input
	V_{IHM}	MD0 to MD3	—	$V_{CC} - 0.3$	—	$V_{CC} + 0.3$	V	
	V_{IHI}	INITX	—	$0.8 \times V_{CC}$	—	$V_{CC} + 0.3$	V	
"L" level input voltage	V_{ILS}	—	—	$V_{SS} - 0.3$	—	$0.5 \times V_{CC}$	V	CMOS automotive input
	V_{ILC}	—	—	$V_{SS} - 0.3$	—	$0.3 \times V_{CC}$	V	CMOS Schmitt input
	V_{ILM}	MD0 to MD3	—	$V_{SS} - 0.3$	—	$V_{SS} + 0.3$	V	
	V_{ILI}	INITX	—	$V_{SS} - 0.3$	—	$0.2 \times V_{CC}$	V	
Power supply current	I_{CC}	VCC	*1	—	40	60	mA	Normal operation *7
			Ta = + 25 °C	—	2	3	mA	PLL stop operation (2 MHz)
			Ta = + 105 °C	—	2.6	4	mA	
	I_{CCS}	VCC	*2	—	28	42	mA	SLEEP operation *7
	I_{CCL}	VCC	*3	—	150	300	µA	Sub-operation *7
	I_{CCR32}	VCC	*4	—	80	200	µA	32 kHz clock operation
	I_{CCR4}	VCC	*5	—	800	1200	µA	4 MHz clock operation
	I_{CCH}	VCC	*6	—	70	150	µA	STOP
Input leakage current	I_{IL}	—	—	− 5	—	+ 5	µA	All input pins
Input capacity	C_{IN}	—	—	—	5	15	pF	
Pull-up resistance	R_{UP}	—	—	25	50	100	kΩ	All ports and INITX
Pull-down resistance	R_{DOWN}	—	—	25	50	100	kΩ	All ports, MD3, MD2*8
Output H voltage	V_{OH}	—	I_{OH}= − 2 mA	$V_{CC} - 0.5$	—	—	V	All ports
Output L voltage	V_{OL}	—	I_{OL}=2 mA	—	—	0.4	V	All ports

*1 : CLKB = 40 MHz, CLKP = 20 MHz, CLKT = 10 MHz, CANCLK = 10 MHz

*2 : Under *2, CPU stopped.

*3 : CLKB = CLKP = CLKT = CANCLK = 32 kHz, Ta = + 25 °C

*4 : CPU/peripheral circuit operation stopped, main oscillation stopped, 32 kHz clock operation, Ta = + 25 °C

*5 : CPU/peripheral circuit operation stopped, sub-oscillation stopped, 4 kHz clock operation, Ta = + 25 °C

*6 : CPU/peripheral circuit operation stopped, all oscillation circuits stopped, Ta = + 25 °C

*7 : The current consumption in normal operation/SLEEP mode, is the value at the maximum operation of the peripheral circuit.

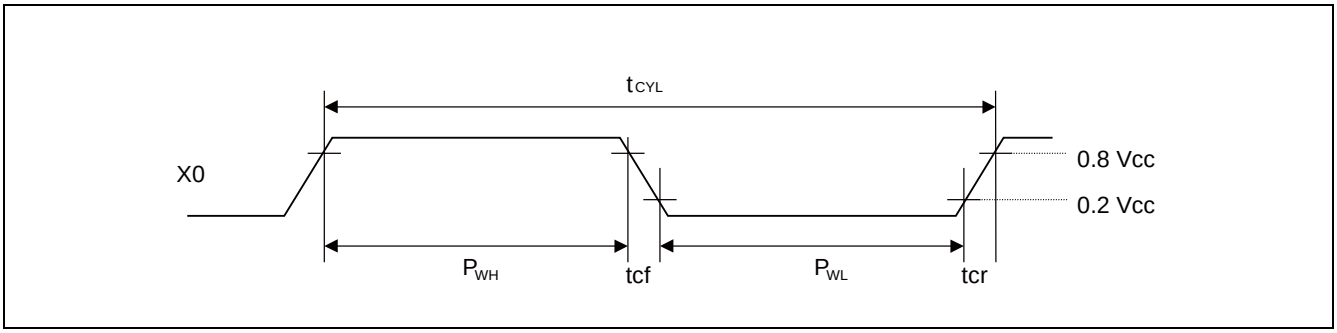
*8 : Only MB91213A

4. AC Specifications

(1) Clock timing

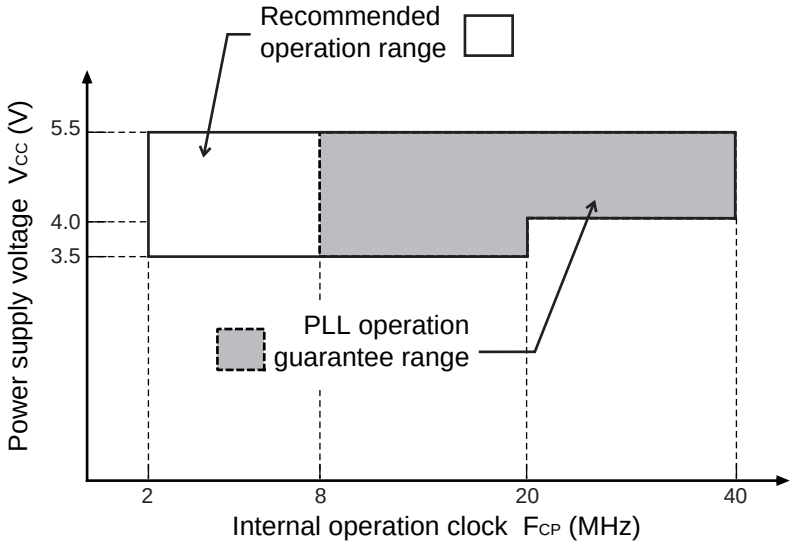
(Ta: Recommended operating conditions; V_{CC} = 5.0 V ±10%, V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Frequency of source oscillation clock	F_C	X0, X1	—	—	4	16	MHz	
	F_{CA}	X0A, X1A		—	32.768	100	kHz	MB91213A/F213A/ F218S
				—	32.768	—	kHz	MB91F211B
Source oscillation clock cycle time	t_{CYL}	X0, X1		62.5	250	—	ns	
	t_{CYLL}	X0A, X1A		10	30.5	—	µs	
Input clock pulse width	P_{WH}, P_{WL}	X0		30	—	—	ns	The duty ration normally ranges from 40% to 60%.
Input clock rise/ fall time	tcr, tcf	X0		—	—	5	ns	When external clock is used
Frequency of internal clock operation	F_{CP}	—		—	—	40	MHz	When main clock and PLL clock is used.
Internal operation clock cycle time	t_{CP}	—	—	25	—	—	ns	When main clock and PLL clock is used.



• **Operation guarantee range**

Relation between internal operation clock frequency and power supply voltage



Note : PLL operation stabilizing wait time should be set to 600 µs or more.

Relation between oscillation clock frequency and internal operation clock (example)

Source oscillation (4 MHz)

Divider	1/2	1/4	1/8
Multiplier	F_{CP}	F_{CP}	F_{CP}
1	–	–	–
2	–	–	8 MHz
4	–	16 MHz	16 MHz
6	–	24 MHz	–
8	32 MHz	32 MHz	–
10	40 MHz	–	–

Source oscillation (5 MHz)

Divider	1/2	1/4	1/8
Multiplier	F_{CP}	F_{CP}	F_{CP}
1	–	–	–
2	–	–	10 MHz
4	–	20 MHz	–
6	–	30 MHz	–
8	40 MHz	–	–
10	–	–	–

Source oscillation (10 MHz)

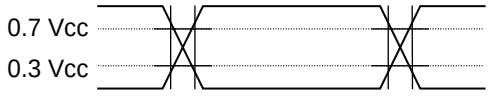
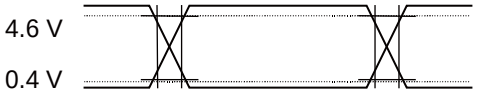
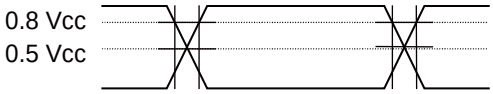
Divider	1/2	1/4	1/8
Multiplier	F_{CP}	F_{CP}	F_{CP}
1	–	–	10 MHz
2	–	20 MHz	–
4	40 MHz	–	–
6	–	–	–
8	–	–	–
10	–	–	–

Source oscillation (16 MHz)

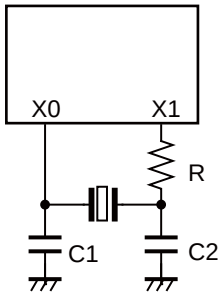
Divider	1/2	1/4	1/8
Multiplier	F_{CP}	F_{CP}	F_{CP}
1	–	16 MHz	16 MHz
2	32 MHz	32 MHz	–
4	–	–	–
6	–	–	–
8	–	–	–
10	–	–	–

–: Prohibited

AC specifications are defined by the following measurement standard voltage values:

Input signal waveform	Output signal waveform
Hysteresis input pin 	Output pin 
Hysteresis input pin (Automotive) 	

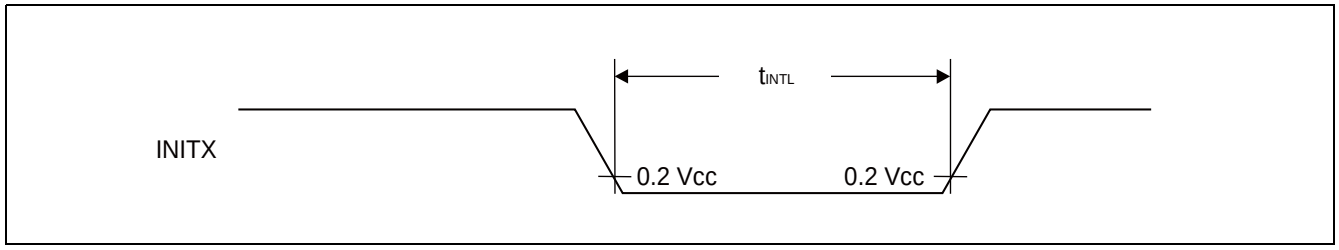
Example oscillation circuit



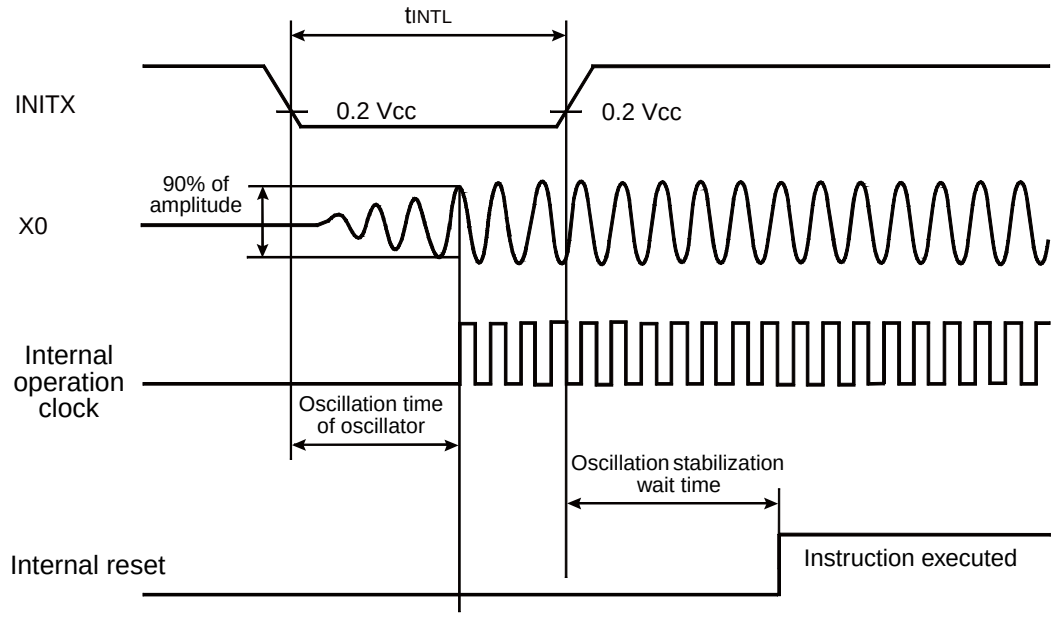
(2) Reset input

(Ta: Recommended operating conditions; V_{CC} = 5.0 V ± 10%, V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
INITX input time	t_{INTL}	INITX	—	500	—	ns	
				$2^{17} \times t_{CYL}$	—	ms	Upon power-on and in stop mode



- In stop mode

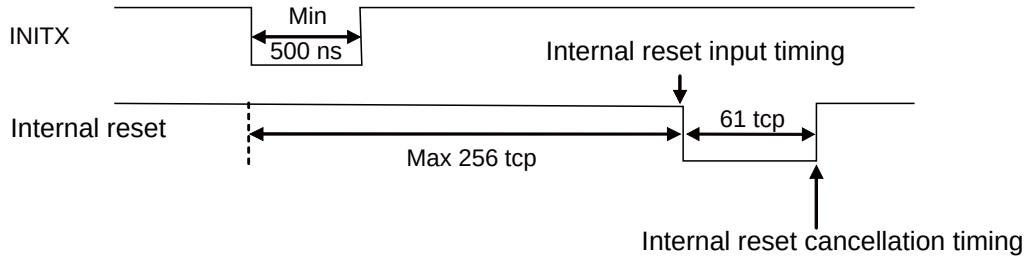


[External reset input specifications (INITX) and internal reset signal cancellation timing]

- When an external reset input is generated, a maximum of 256 tcp is designed to be spent until it reaches the internal reset signal to transmit all reset signals to the internal logic.
  (Max 6.4 µs at 40 MHz)
- The following chart shows how to set the timing for instruction execution start (start of application operation) after external reset input.

  Time from external reset input to instruction start = Max 256 tcp + 61 tcp

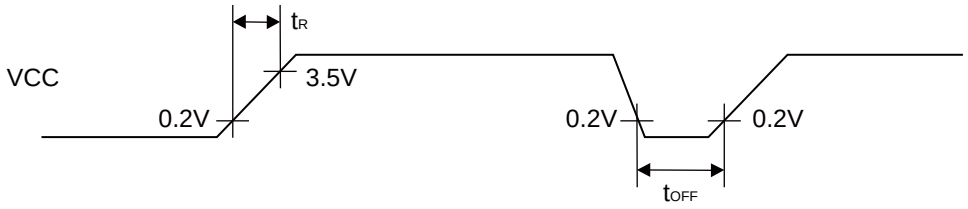
- Timing Chart



(3) Power-on Conditions

(Ta : Recommended operating conditions; V_{SS} = 0.0 V)

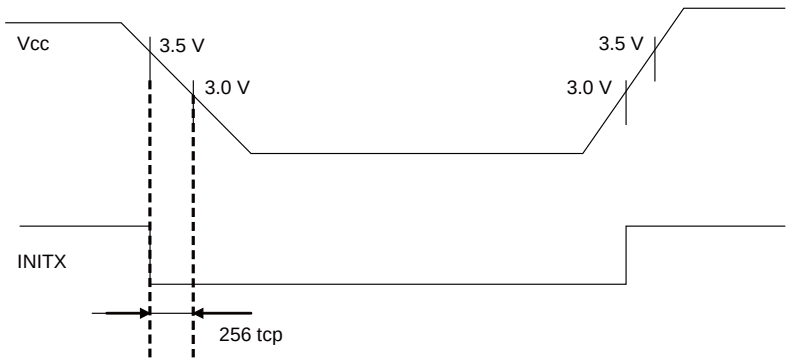
Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
Power supply rising time	t_R	VCC	—	0.05	30	ms	—
Power supply start voltage	V_{OFF}			—	0.2	V	—
Power supply peak voltage	V_{ON}			3.5	—	V	—
Power supply cut-off time	t_{OFF}			50	—	ms	Due to repetitive operation



(4) Power supply drop time, power supply voltages and external reset input to retain RAM data.

Satisfy the following reset input standard to retain the RAM data used in the single chip mode.

V_{CC}(V)	Voltage drop time	External reset input standard (INITX)
3.5 V → 3.0 V dropped	Min 256 tcp	Min 256 tcp



To retain RAM data, enter 256 tcp of INITX or more before dropping V_{CC} to 3.0 V or lower.

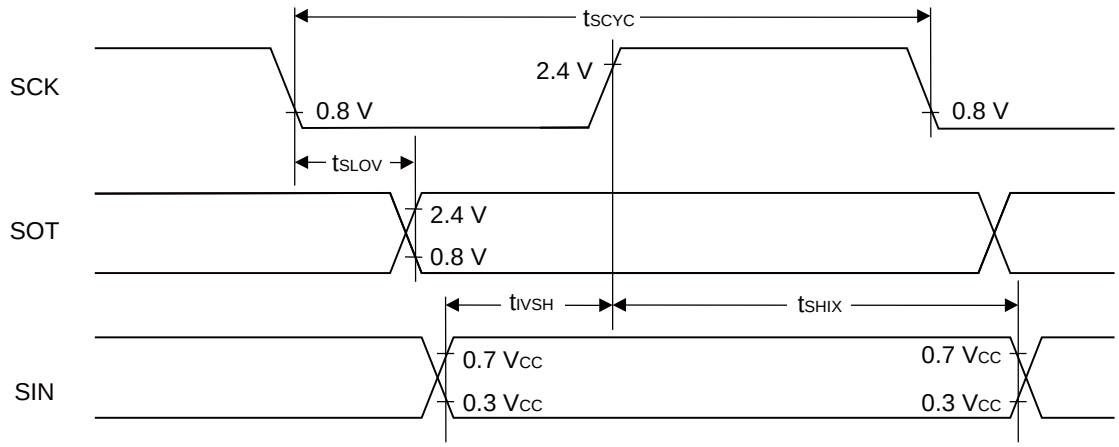
(5) UART Timing

(Ta: Recommended operating conditions; V_{CC} = 5.0 V ± 10%, V_{SS} = AV_{SS} = 0.0 V)

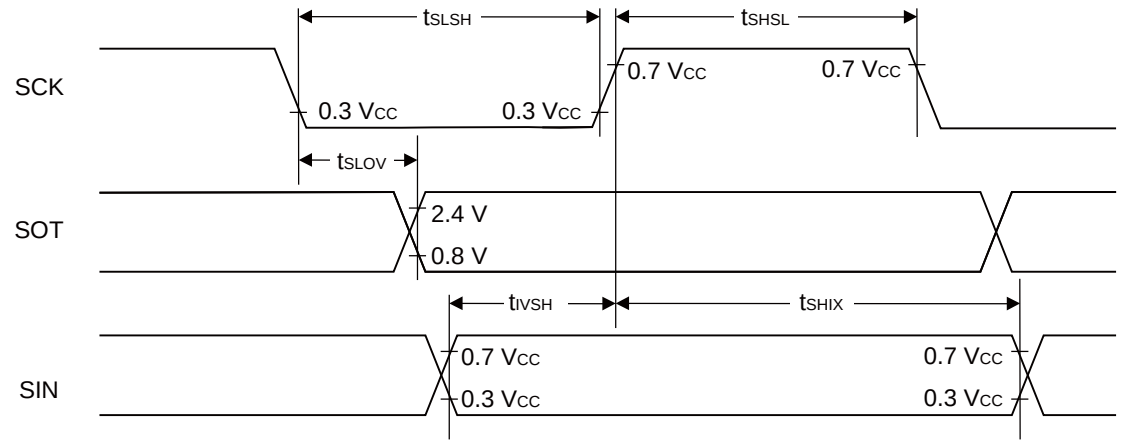
Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK	Output pin, C_L = 30 pF + 1 × TTL	8 t_{CP}	—	ns	For internal shift clock mode
SCK ↓ → SOT delay time	t_{SLOV}	SCK SOT		− 80	+ 80	ns	
Valid SIN → SCK ↑	t_{IVSH}	SCK SIN		100	—	ns	
SCK ↑ → Valid SIN hold time	t_{SHIX}			60	—	ns	
Serial clock “H” pulse width	t_{SHSL}	SCK	Output pin, C_L = 30 pF + 1 × TTL	4 t_{CP}	—	ns	For external shift clock mode
Serial clock “L” pulse width	t_{SLSH}			4 t_{CP}	—	ns	
SCK ↓ → SOT delay time	t_{SLOV}	SCK SOT		—	2 × CLKP + 60	ns	
Valid SIN → SCK ↑	t_{IVSH}	SCK SIN		60	—	ns	
SCK ↑ → Valid SIN hold time	t_{SHIX}			60	—	ns	

Note: These are AC characteristics for CLK synchronous mode.
C_L is a load capacitance connected to pins during testing.

- For internal shift clock mode



- For external shift clock mode

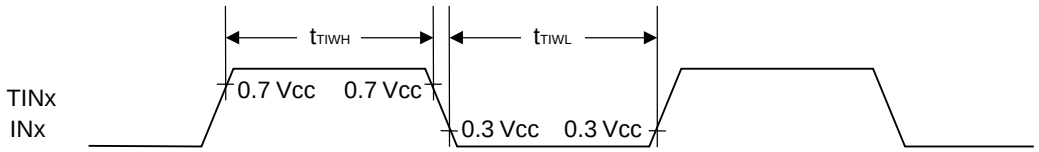


(6) Timer Input Timing

(Ta: Recommended operating conditions; V_{CC} = 5.0 V ± 10%, V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Input pulse width	t_{TIWH} t_{TIWL}	TIN0 to TIN2 IN0 to IN7	—	4 t_{CP}	—	ns

- Timer Input Timing

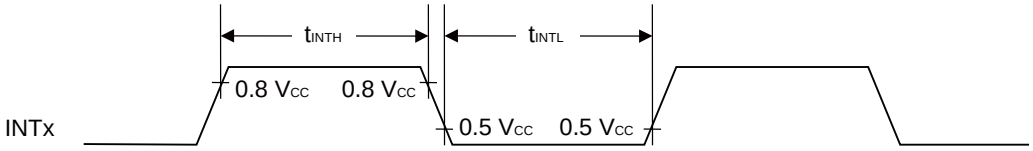


(7) External Interrupt Timing

(Ta: Recommended operating conditions; V_{CC} = 5.0 V ± 10%, V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Input pulse width	t_{INTH}, t_{INTL}	INT0 to INT15	—	3 t_{CP}	—	ns
			STOP mode	1.0	—	µs

- External Interrupt Input Timing



5. Flash Memory Write/Erase Characteristics

Parameter	Condition	Value			Unit	Remarks
		Min	Typ	Max		
Sector erase time	—	—	0.9	3.6	s	Exclusive of internal write time prior to erase
Word write time	—	—	23	370	µs	Exclusive of overhead time at system level
Chip write time	—	—	6.2	102	s	Exclusive of overhead time at system level
Erase/write cycle	—	10000	—	—	cycle	
Data retention time	Average Ta= + 85 °C	20*	—	—	year	

*: This value comes from the technology qualification (using Arrhenius equation to translate high temperature measurements into normalized value at + 85 °C).

6. A/D Converter Electrical Characteristics

(Ta : Recommended operating conditions; V_{CC} = 3.5 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	—	—	—	—	10	bit	
Total error	—	—	—	—	± 3.0	LSB	
Non-liner error	—	—	—	—	± 2.5	LSB	
Differential linearity error	—	—	—	—	± 1.9	LSB	
Zero transition voltage	V_{OT}	AN0 to AN31	AV_{SS} – 1.5LSB	AV_{SS} + 0.5LSB	AV_{SS} + 2.5LSB	V	1LSB = (AVRH-AV_{SS})/1024
Full-scale transition voltage	V_{FST}	AN0 to AN31	AVRH – 3.5LSB	AVRH – 1.5LSB	AVRH + 0.5LSB	V	
Sampling time	t_{SMP}	—	1.1	—	—	µs	V_{CC} = AV_{CC} = 4.5 V to 5.5 V*1
			1.65	—	—	µs	V_{CC} = AV_{CC} = 3.5 V to 4.5 V*5
Compare time	t_{CMP}	—	1.1	—	—	µs	V_{CC} = AV_{CC} = 4.5 V to 5.5 V*2
			2.2	—	—	µs	V_{CC} = AV_{CC} = 3.5 V to 4.5 V*6
A/D conversion time	t_{CNV}	—	2.2	—	—	µs	V_{CC} = AV_{CC} = 4.5 V to 5.5 V*3
			3.85	—	—	µs	V_{CC} = AV_{CC} = 3.5 V to 4.5 V*7
Analog port input current	I_{AIN}	AN0 to AN31	—	—	10	µA	$V_{AVSS} \le V_{AIN} \le V_{AVCC}$
Analog input voltage	V_{AIN}	AN0 to AN31	0	—	AVRH	V	
Standard voltage	AVRH	AVRH	4.0	—	AV_{CC}	V	
Power supply current	I_A	AVCC	—	2.4	4.7	mA	
	I_{AH}		—	—	5	µA	*4
Standard voltage supply current	I_R	AVRH	—	600	900	µA	V_{AVRH} = 5.0 V
	I_{RH}		—	—	5	µA	*4
Variation between channels	—	AN0 to AN31	—	—	4	LSB	

*1 : When F_{CP} is 40 MHz : t_{SMP} = (Rext + Rin) × Cin × 7 = ST × CLKP cycle = 2 Ch × 25 ns = 1.1 µs

*2 : When F_{CP} is 40 MHz : t_{CMP} = CKIN × 11 = CT × CLKP cycle × 11 = 4 h × 25 ns × 11 = 1.1 µs

*3 : This represents the conversion time per channel when t_{SMP} and t_{CMP} are selected while F_{CP} is 40 MHz.

(Continued)

(Continued)

*4: This defines the power supply current when the A/D converter is not in operation and the CPU is stopped (at "V_{CC} = AV_{CC} = AVRH = 5.0 V")

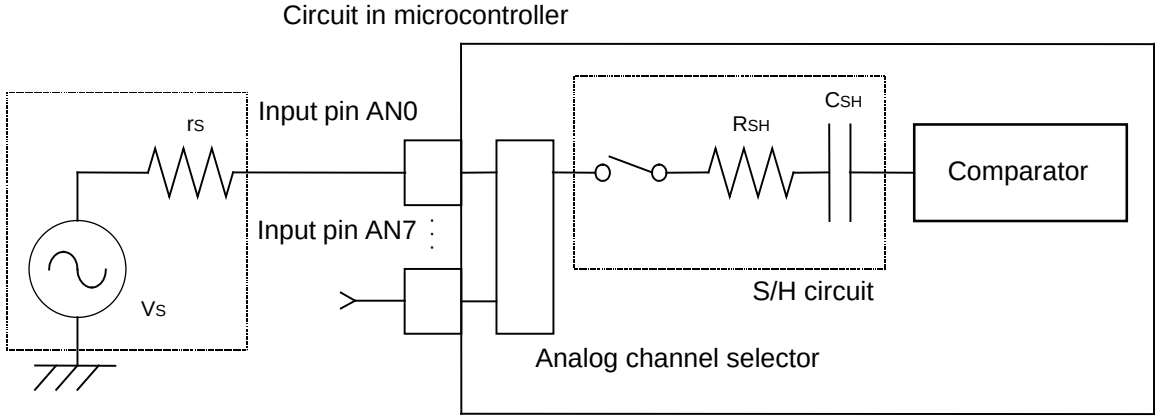
*5 : When F_{CP} is 20 MHz : $t_{SMP} = (R_{ext} + Rin) \times Cin \times 7 = ST \times CLKP$ cycle = 21h × 50 ns = 1.65 µs.

*6 : When F_{CP} is 20 MHz : $t_{CMP} = CKIN \times 11 = CT \times CLKP$ cycle × 11 = 4 h × 50 ns × 11 = 2.2 µs.

*7 : This represents the conversion time per channel when t_{SMP} and t_{CMP} are selected while F_{CP} is 20 MHz.

Notes:
- As AVRH becomes smaller, the error becomes greater.
- Use the output impedance r_S of the external circuit for analog input under the following conditions : Output impedance r_S of the external circuit = 4 kΩ (Max)
- If the output impedance of the external circuit is too high, the sampling time of the analog voltage may not be sufficient.
- When placing a DC blocking capacitor between the external circuit and input pin, set the capacitance to the value calculated by multiplying C_{SH} by several thousands as a guideline in order to minimize the impact from dividing voltage capacitance with C_{SH}.

• Analog Input Equivalent Circuit



<Recommended parameter values and tentative guideline for each element>
r_S 4 kΩ or less
R_{SH} = approx. 2.5 kΩ (5 V ± 10%)
C_{SH} = approx. 8.5 pF
Note: These element parameters should be regarded as tentative values used only for design purposes.

■ TERM DEFINITIONS

Resolution

Level of analog variation that can be distinguished by the A/D converter.
When the number of bits is 10, the analog voltage can be resolved into 2^{10} = 1024.

Total error

Difference between actual and theoretical values, which is a total value derived from an offset error, gain error, non-linearity error and noise.

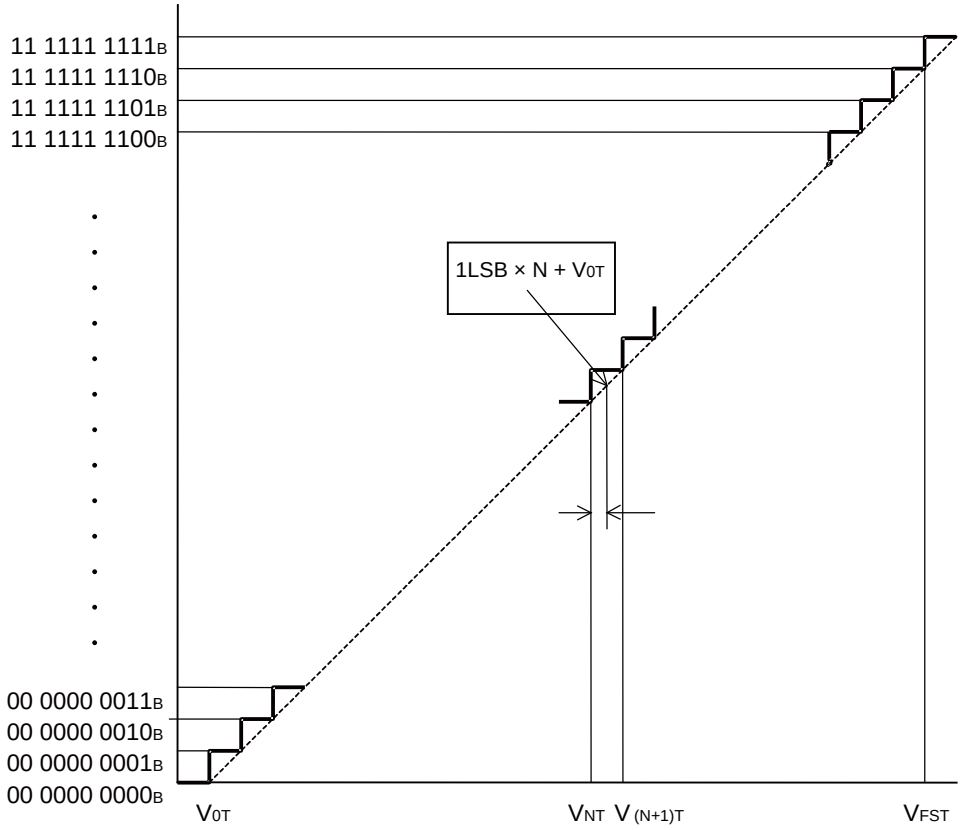
Linearity error

Deviation between the value along a straight line connecting the zero transition point
(“00 0000 0000” ⟷ “00 0000 0001”) of a device and the full-scale transition point
(“11 1111 1110” ⟷ “11 1111 1111”) compared with the actual conversion values obtained.

Differential linearity error

Deviation of input voltage, which is required for changing output code by 1 LSB, from an ideal value.

- 10-bit A/D Converter- Conversion Characteristics



N = A/D converter digital output value.
V_{0T} = AVss + 0.5LSB [V] (Theoretical value)
V_{FST} = AVRH 1.5LSB [V] (Theoretical value)
V_{NT}: Transition voltage of digital output from $(N-1)_H$ to N_H

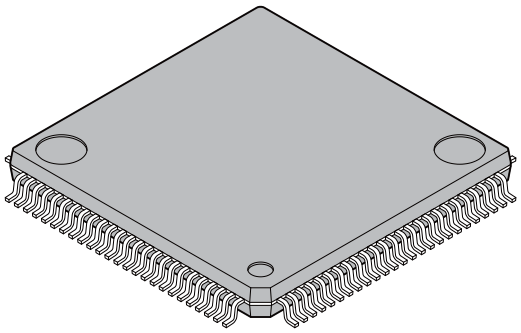
$$\text{Linearity error} = \frac{V_{NT} - (1LSB \times N + VOT)}{1LSB} \text{ [LSB]}$$

$$\text{Differential linearity error} = \frac{V_{(N+1)T} - V_{NT}}{1LSB} - 1 \text{ [LSB]}$$

■ ORDERING INFORMATION

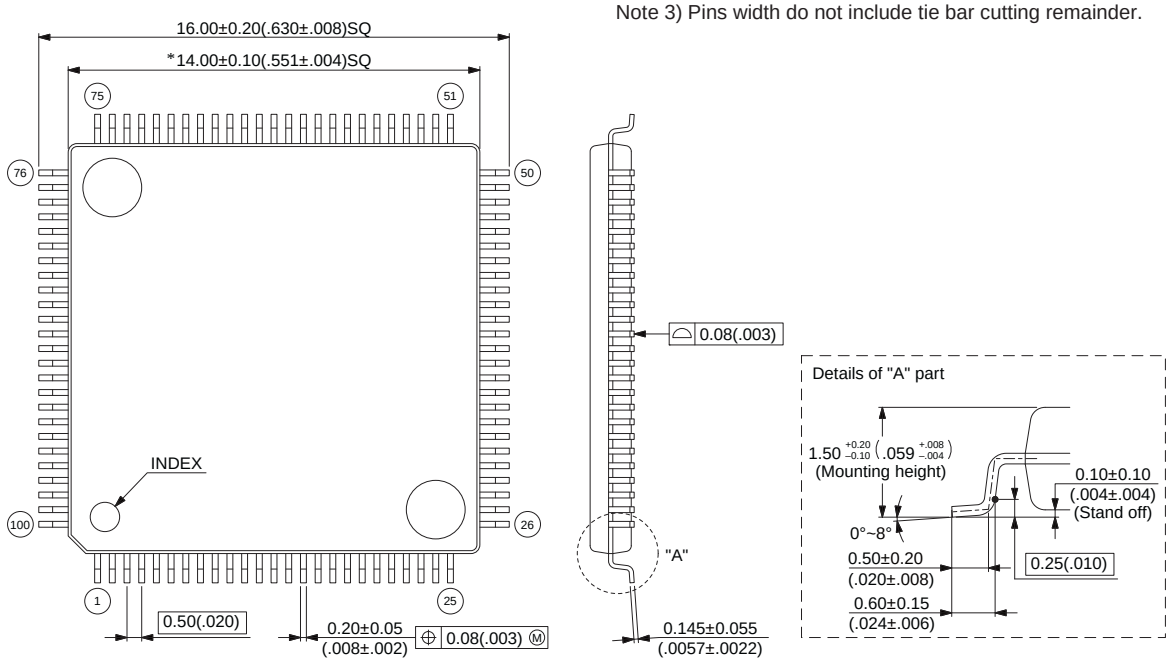
Part No.	Package
MB91F211BPMC-GSE1	100-pin plastic LQFP (FPT-100P-M20)
MB91213APMC-GSE1	144-pin plastic LQFP (FPT-144P-M08)
MB91F213APMC-GSE1	144-pin plastic LQFP (FPT-144P-M08)
MB91F218SPMC-GTE1	144-pin plastic LQFP (FPT-144P-M08)
MB91V210PB-ESE1	420-pin plastic PBGA (BGA-420P-M01)

■ PACKAGE DIMENSION

100-pin plastic LQFP		
	Lead pitch	0.50 mm
	Package width × package length	14.0 mm × 14.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm Max
	Weight	0.65 g
(FPT-100P-M20)	Code (Reference)	P-LFQFP100-14×14-0.50

100-pin plastic LQFP
(FPT-100P-M20)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values

Please confirm the latest Package dimension by following URL.
http://edevice.fujitsu.com/package/en-search/

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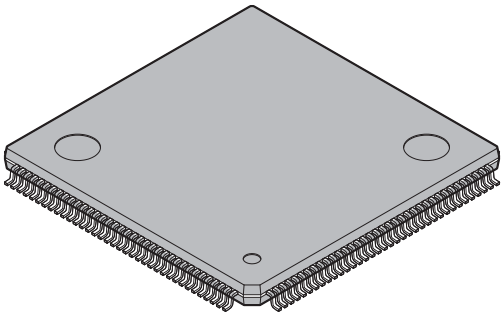
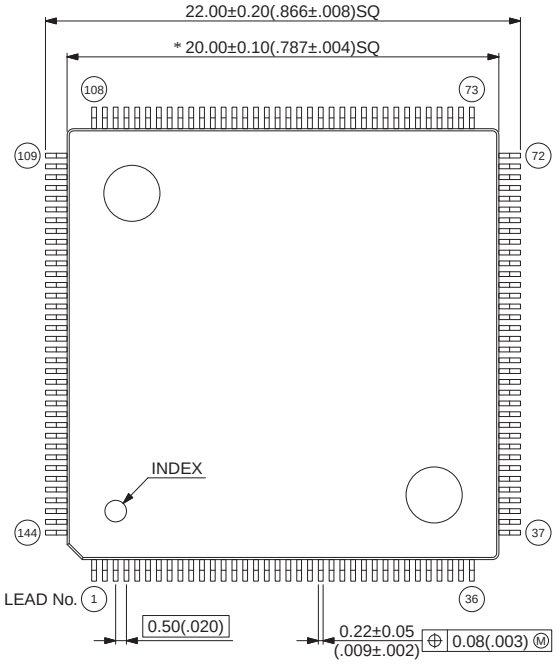
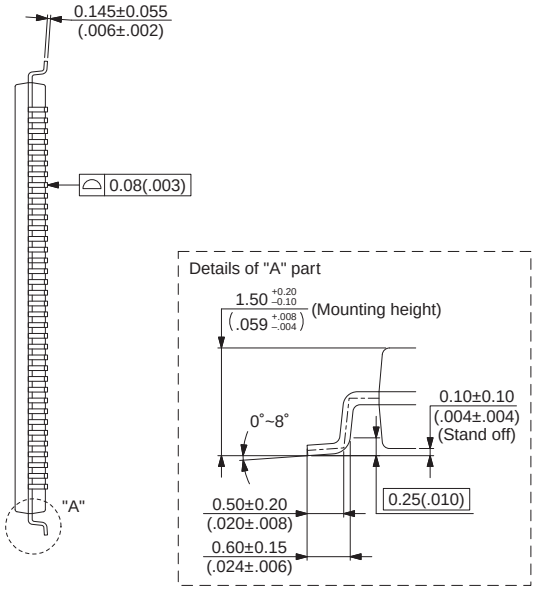
144-pin plastic LQFP		
	Lead pitch	0.50 mm
	Package width × package length	20.0 × 20.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Weight	1.20g
(FPT-144P-M08)	Code (Reference)	P-LFQFP144-20×20-0.50

144-pin plastic LQFP
(FPT-144P-M08)



Note 1) *:Values do not include resin protrusion.
Resin protrusion is +0.25(.010)Max(each side).
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

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■ MAIN CHANGES IN THIS EDITION

Page	Section	Change Results
17	■ HANDLING DEVICES	Added the item of “• Serial Communication”
21	■ MODE SETTINGS	Corrected the figure of “Detailed description of mode data” bit31, bit30, bit29, bit28, bit27, bit26, bit25, bit24 → bit7, bit6, bit5bit4, bit3, bit2, bit1, bit0

The vertical lines marked in the left side of the page show the changes.

FUJITSU MICROELECTRONICS LIMITED

Shinjuku Dai-Ichi Seimei Bldg., 7-1, Nishishinjuku 2-chome,
Shinjuku-ku, Tokyo 163-0722, Japan
Tel: +81-3-5322-3347 Fax: +81-3-5322-3387
http://jp.fujitsu.com/fml/en/

For further information please contact:

North and South America
FUJITSU MICROELECTRONICS AMERICA, INC.
1250 E. Arques Avenue, M/S 333
Sunnyvale, CA 94085-5401, U.S.A.
Tel: +1-408-737-5600 Fax: +1-408-737-5999
http://www.fma.fujitsu.com/

Europe
FUJITSU MICROELECTRONICS EUROPE GmbH
Pittlerstrasse 47, 63225 Langen, Germany
Tel: +49-6103-690-0 Fax: +49-6103-690-122
http://emea.fujitsu.com/microelectronics/

Korea
FUJITSU MICROELECTRONICS KOREA LTD.
206 Kosmo Tower Building, 1002 Daechi-Dong,
Gangnam-Gu, Seoul 135-280, Republic of Korea
Tel: +82-2-3484-7100 Fax: +82-2-3484-7111
http://kr.fujitsu.com/fmk/

Asia Pacific
FUJITSU MICROELECTRONICS ASIA PTE. LTD.
151 Lorong Chuan,
#05-08 New Tech Park 556741 Singapore
Tel : +65-6281-0770 Fax : +65-6281-0220
http://www.fmal.fujitsu.com/

FUJITSU MICROELECTRONICS SHANGHAI CO., LTD.
Rm. 3102, Bund Center, No.222 Yan An Road (E),
Shanghai 200002, China
Tel : +86-21-6146-3688 Fax : +86-21-6335-1605
http://cn.fujitsu.com/fmc/

FUJITSU MICROELECTRONICS PACIFIC ASIA LTD.
10/F., World Commerce Centre, 11 Canton Road,
Tsimshatsui, Kowloon, Hong Kong
Tel : +852-2377-0226 Fax : +852-2376-3269
http://cn.fujitsu.com/fmc/en/

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