

FEATURES

- DC coupled and terminated PECL inputs
- AC coupled PECL outputs
- Programmable via any PC using printer cable
- Includes a 27.0000MHz oscillator on board

EVALUATION BOARD COMPONENTS

- SY87729/39L evaluation board
- SY87729/39L data sheet and this document
- SY87729/39L software (download from http://www.micrel.com/product-info/ fractional_n_synthesizers.shtml)
- Two length-matched 1 foot SMA cables (optional, user supplied)
- PC running Windows (user supplied)
- Printer cable, parallel-to-centronics (user supplied)

DESCRIPTION

The SY87729/39L are rate independent fractional-N frequency synthesizer ICs. From a single reference source, they can generate any clock frequency from 10MHz to 729MHz very accurately.

This document provides a detailed description of the evaluation board, evaluation procedure and the simple configuration software it uses. Complete information in this document includes:

- 1. Test setup and measuring frequency output with a signal generator.
- 2. Test setup and measuring jitter with an internal reference oscillator.
- 3. Download and use of the configuration software
- 4. Board schematic and Bill of Materials.



GETTING STARTED

Before powering up the SY87729/39L evaluation board, you must do the following:

- 1. Familiarize yourself with the SY87729/39L evaluation board.
- 2. Make sure that you are properly grounded.
- 3. Read and understand this document in its entirety.

To program the desired output frequency, you will need a PC running Windows, with the SY87729/39L evaluation board software installed, and a printer cable attached between the PC and the SY87729/39L evaluation board. The software downloads configuration information to the SY87729/39L device.

If using an external signal source, that source must be able to generate LVPECL level signals. The inputs are DC coupled, terminated in 50Ω to V_{CC}-2V.



Figure 1. Test Set-Up with Signal Generator

TEST SET-UP

This section discusses how to make two common measurements with the SY87729/39L evaluation board.

What you will need:

- 1. The SY87729/39L evaluation board.
- 2. Either two length-matched one foot SMA cables, or a digital signal generator such as the HP8133A.
- 3. A PC with a parallel port, running Windows.
- 4. If you are running Windows NT, Windows 2000, or Windows XP, you will need "Direct-IO" shareware.
- 5. A printer cable, one end is a parallel interface, the other end is a Centronics interface.
- 6. The SY87729/39L evaluation board software (download from http://www.micrel.com).
- 7. A frequency counter.
- 8. A power supply capable of delivering at least 3.3V at 0.5A.
- 9. A self-triggering scope or a time interval analyzer (TIA).

First, we show how to use an external signal generator and how to measure the frequency of the output. Second, we show how to use the supplied reference oscillator and how to measure cycle-to-cycle jitter of the output. Please refer to Figures 1 and 2.



Figure 2. Test Set-Up with Internal Reference Oscillator

EVALUATION PROCEDURE

Downloading the Application Software

Micrel's SY87729/39L accepts configuration information via a bit-serial interface. To program the device, the user must download 32 bits of configuration information into SY87729/39L. Micrel provides a download application for use with the SY87729/39L evaluation board.

With this software, the user may select any desired output frequency that the SY87729/39L can generate, between 10MHz and 729MHz. The software will automatically determine the configuration parameters that most accurately generate the desired frequency. These parameters, explained in the data sheets, may be viewed or modified. They may also be downloaded to the SY87729/39L-EVAL circuit board through a printer cable attached between the PC and the SY87729/39L evaluation board.

To download the software, point your web browser to the following URL, and save the files to your PC: You should download the applications "739ifier", "739ev" and "739ev2."

http://www.micrel.com/page.do?page=product-info/ fractional_n_synthesizers.shtml

Installing the Application Software

Create a folder just for these applications. Download all three application files into this folder.

Running Win95, Win98, or WinME

If you are running any of these Windows operating systems, you have completed downloading all the software you will need. You will not need the application file "739ev2" and may delete it at your convenience. The application file "739ev" allows you to access one of two parallel ports, the default one located at base I/O address 0x378 (usually known as LPT1) and a secondary one located at base I/O address 0x278 (usually known as LPT2).

The application program "739ev2" is identical to application file "739ev", except that it defaults to using LPT2 first. This is of no use to the user when running Win95, Win98, or WinME. Please proceed to the section "Using the Application Software."

Running WinNT, Win2000, or WinXP

Besides downloading the applications, you must also decide what parallel port or ports you will use the applications with. Since WinNT, Win2000, and WinXP do not permit direct access to the I/O ports, you must also download and install a shareware to allow this.

The usual case is to allow downloads on the default parallel port, LPT1. You may instead decide to allow downloads only on LPT2, if your computer is equipped with a second parallel port or you may also decide to allow two SY87729/39L-EVAL boards to be attached, one to each LPT1 and LPT2. Table 1 details the I/O ports you must allow access to, based on which parallel port or ports you will use with SY87729/39L evaluation board.

Case	Base I/O Addresses Needed
Access to LPT1	0x378-0x37A, 0x778-0x77A
Access to LPT2	0x278-0x27A, 0x678-0x67A
Access to both LPT1 and LPT2	0x278-0x27A, 0x378-0x37A, 0x678-0x67A, 0x778-0x77A

Table 1. I/O Addresses to Use

Once you have decided which parallel port or ports you will connect the SY87729/39L evaluation board to, you must choose which download application file to keep. If you will access either LPT1 only, or both LPT1 and LPT2, then delete the application "739ev2" at this time. If you will access only LPT2, then delete the application "739ev2" at this time, and then rename the application "739ev2" to "739ev."

Now, you must download a shareware called "Direct-IO" that allows the SY87729/39L evaluation board software application access to the parallel ports at a low level. The "Direct-IO" shareware is available at:

http://www.direct-io.com

At the time of this writing, you have a free 30-day trial evaluation period, after which time you must have it registered. After you have completed download of "Direct-IO," you must install the program. Follow the installation instructions for that program. Please note that, in some cases, the install may fail. In this case, you will need a systems administrator to install "Direct-IO" for you.

As the final step of application installation, you must configure "Direct-IO" to give the SY87729/39L evaluation board software permission to access to the appropriate I/O addresses. This is accomplished through its control panel. To access the "Direct-IO" control panel, select:

Start \Rightarrow Programs \Rightarrow Direct IO \Rightarrow Control Panel

If not already active, click the "I/O Ports" tab. The "Hex" button should already be pressed. You must enter the appropriate address ranges in the "Begin" and "End" edit boxes, and then push the "Add" button. The goal is to have the required I/O addresses appear in the "Active Ports" section of the "Direct-IO" control panel. For example, to allow access only to LPT1, you must allow access to two ranges of I/O addresses. The first range is 0x378-0x37A. Thus, you type "378" in the "Begin" edit box, and you type "37A" in the "End" edit box. The "Direct-IO" control panel should look like Figure 3.

VO Ports IROs M	mary Security	Into	
Active Borts:		Begin: 37 End: 37	18 14 Heg Dec Add
	OK	Cencel	Help

Figure 3. Filling in the I/O Ports Tab

You then click the "Add" button. This selects the range of I/O addresses specified, and places it into the "Active Ports" Window, as shown in Figure 4.

			88
VO Ports IRQs Mor	many Security	Into	
Active Borts:		Begin:	
378-37A		End:	
		He	<u>Dec</u>
			695
			3/12/12
	OK	Cancel	Help

Figure 4. After pressing the "Add" Button

To continue with this example, the SY87729/39L evaluation board application also needs access to I/O addresses 0x778 through 0x77A. Thus, type "778" in the "Begin" edit box, and type "77A" in the "End" edit box. Then click the "Add" button. The "Direct-IO" control panel should look like Figure 5.

VO Ports IROs	tings Memory Security	linto	3
Active Borts: 378 - 37A 778 - 77A		End: Heg Dec	
		Add Beneve	
	ОК	Cancel Help	



Consulting Table 1, If you are accessing only LPT2, the "Direct-IO" control panel should look like Figure 6.

Active Borts:	1	Begin: [
278 - 27A 678 - 67A		End:	
		Γ	Heg Dec
			<u>(</u> 155

Figure 6. Correct I/O Addresses for LPT2 Access

Finally, to access both LPT1 and LPT2, the "Direct-IO" control panel should look like Figure 7.

[∞] Direct I/O Set	tings		2 🛛
VO Ports IROs	Memory Security	Into	
Active Borts: 278 - 27A 378 - 37A		Begin:	_
678 - 67A. 778 - 77A.			Heg Dec
			Berrave
	OK	Cancel	Help

Figure 7. Correct I/O Addresses for both LPT1 and LPT2 Access

After entering the I/O addresses to allow access to, you must specify the program or programs allowed to access these I/O locations. Click the "Security" tab. Click the "Browse..." button. Select the directory into which you placed the SY87729/39L evaluation board application programs, and select the application, "739ev." The path and application will appear in the "Allowed Processes:" edit box. Click the "Add" button to include "739ev" in the list of allowed programs. The "Direct-IO" control panel should look like Figure 8, except that the path will be whatever you chose.

Manual Processor:	
	Browse_
C:\WINNT\Profiles\vanscherrenburgM\De: <u></u>	Astr
	Benzie
-	More

Figure 8. Including "739ev" in the List of Allowed Processes

Click the "OK" button. Check your work by running the "739ev" application. If, instead of running, you get a message box like that in Figure 9, you've performed one or more of the above steps incorrectly. Re-read this section carefully, and try again.



Figure 9. Error Message if "Direct-IO" Incorrectly Installed

Using the Application Software

The application software consists of two components, a calculation module "739ifier", and a download module, "739ev." There can be only one instance of the download module running at any given time, but there can be any number of instances of the calculation module running, easing testing at multiple frequencies.

Using the Calculation Module:

The parts of the calculation module appear in Figure 10 below.



Figure 10. The Calculation Module

The purpose of the calculation module is to ease the burden on the designer using SY87729/39L. Instead of manually figuring out the configuration values, the calculation module will determine the optimal configuration parameters, based on three inputs.

The calculation module accepts these three inputs, and displays several outputs. The first input accepted is the reference frequency of the clock being provided to the SY87729/39L. This goes in the "Reference" edit box. When starting an instance of the calculation module, this edit box is preset to 27MHz, the frequency Micrel recommends when synthesizing clocks for standard protocols. This also happens to be the frequency of the on-board reference oscillator provided with the SY87729/39L evaluation board. Should the user wish to use a different reference frequency, type it in here.

A note on entering data in the "Reference" or "739 Output" edit boxes. To ease typing, you may use the suffix "m" or "k" for "mega" or "kilo" respectively. For example, to type in 27MHz, you can strike the following keys: "2", "7", and "m".

The second input is the user's decision whether or not to reserve the wrapper synthesizer on the SY87729/39L. In most circumstances, the wrapper synthesizer should be used. That is why the calculation module starts with the "Use" radio button selected in the "Wrapper" group box. This tells the calculation module to use the wrapper synthesizer, if there is some advantage in doing so, to generate the target output frequency.

On the other hand, to reserve the wrapper synthesizer, click on the "Reserve" radio button in the "Wrapper" group box. This tells the calculation module to not use the wrapper synthesizer when generating output frequencies. The "M" and "N" parameters will always be 14, indicating that the wrapper synthesizer is not modifying the output of the fractional-N synthesizer.

As shown later in this document, using the wrapper synthesizer generally results in a better output frequency, smaller frequency error, and lower jitter. An example where the user might wish to reserve (not use) the wrapper synthesizer is in an application where not only several data rates may need to be accepted, but also these data rates may or may not optionally be modified with some FEC or digital wrapper. Perhaps a DWDM input would need to accept a list of possible inputs. But, these may have no FEC, an ITU standard FEC, or a proprietary digital wrapper for each input data rate.

One technique would be to create an initial list of data rates to accept, and from these, a list of desired reference clocks the SY87729/39L would need to generate. From this list, generate a list triple in size. From this new, larger list, type in each frequency and record the SY87729/39L configuration parameters that would generate these.

An alternative would be to reserve the wrapper synthesizer, and then to form a list of configuration parameters for just the base frequencies. The user would then modify just the "M" and "N" parameters to allow without FEC, with FEC, or with digital wrapper.

The third input is the desired output frequency. Please keep in mind that the output frequency range is from 9MHz to 729MHz. Like the input frequency, you can use suffixes. As an example, let's synthesize 8,900,000Hz from a 27MHz input. Launch "739ifier". The input frequency is already set to 27MHz, the wrapper is already set to be used, and the cursor is ready to accept an output frequency. Type "8", ".", "9", and "m". You will get a beep. The status line, the line just below the output frequency, begins with the word FAILED, like in Figure 11. It is VERY IMPORTANT to note that NONE of the SY87729/39L parameters, even if displayed, is valid when the status line begins with either the word FAILED or the word STALE.



Figure 11. Desired Output Frequency Cannot Be Synthesized

The error message is telling you that SY87729/39L cannot synthesize an 8.9MHz clock from a 27MHz clock. Remember, the smallest output frequency SY87729/39L can generate is 9.0MHz, no matter what the input frequency is.

Let's try another example. Suppose we want to generate 111,100,000MHz from 27MHz. Hit the "Tab" key until the output frequency value is highlighted, and then type "1", "1", "1", "1", "1", and "m". Your calculation module should look like that in Figure 12.

am 739 ñer			
Reference 27.001.0	(Hz)	Op	1
		Op-1	22
Actual 111.095.1	(Hz)	P	23
739 Output 11.100.0	000 (Hz)	Post Div	5
SUCCESS - error = I	8 (ppm)	- Oor Day	-
Wrapper	-SY87721L-	M	15
C Reserve	@ Exclude	N	14
@ Use	C Include	721 DivSel	
Celculate	Evit	LiseThe	
0.00010.0			

Figure 12. Generating 111.1MHz With the Wrapper

The status line begins with the word SUCCESS. This means that SY87729/39L can generate the output frequency specified. The closest frequency it can generate is shown in the "Actual" box. In this case, it is 111,099,130MHz, just a bit low. The status line shows that the actual output frequency differs from the desired (or target) output frequency by 8ppm in frequency.

On the far right, the six SY87729/39L configuration parameters to generate this output frequency are shown. These parameters could be used by a firmware engineer to program an embedded processor to configure SY87729/39L.

In the above example, the wrapper synthesizer is used to obtain the best possible actual output frequency. If the wrapper synthesizer is not used, the calculation module should look like that in Figure 13.

≡739iñer			
Reference 27.001.0	(Hz)	Op	20
		Op-1	9
Actual 111.103	.448 (Hz)	P	25
739 Output 111.100	.000 (Hz)	Post Div	6
SUCCESS - error -	32 (ppm)	м	14
@ Reserve	SY87721L @ Exclude	N	14
C Use	C Include	721 DivSel	
Colculate	Exit	Use The	10

Figure 13. Generating 111.1MHz Without the Wrapper

Note that in this example, the "M" and "N" configuration parameters are both 14. This means that the wrapper synthesizer is passing the frequency of the fractional-N synthesizer unchanged. Because of this, the nearest frequency is now 111,103,448Hz, just a bit higher than the target frequency. The status line indicates that the frequency error is now 32ppm, which is not as good as the 8ppm error when the wrapper synthesizer is used.

Let's try another example. Let's generate an OC-12 clock from this 27MHz input frequency. The calculation module should look like that shown in Figure 14. Note that, since the wrapper synthesizer was reserved, both the "M" and the "N" configuration parameters are set to 14.

≡739iñer				
Reference	27.001.000	(Hz)	Op	1
			Op-1	2.4
Actual	622,080,000	(Hz)	P	24
739 Output	622.080.000	(Hz)	Post Div	1
SUCCESS - error = 0 (ppm)		м	14	
-Wrappe @ Rose	r SY8	37721L Exclude	N	14
C Use	01	nclude	721 DivSel	
Calcu	late	Ext	Use The	10

Figure 14. Generating 622.08MHz Without the Wrapper (Using SY87739L only)

Now let's see what happens when you use the wrapper synthesizer. Your calculation module should look like that in Figure 15.

æ≡739ifier				
Reference 27,000,0	00	(Hz)	Op	3
			Op-1	2
Actual 622,080,1	000	(Hz)	P	22
739 Output 622.080.1	000	(Hz)	PostDiv	1
SUCCESS - error =	0 (ppm)		м	15
C Reserve	SY8772 @ Exclu	1L	N	16
	C Inclu	de	721 DivSel	
Calculate	Ex	it .	Use Thes	0

Figure 15. Generating 622.08MHz With the Wrapper (Using SY87739L Only)

In both Figures 14 and 15, the output frequency was generated exactly. However, generated jitter tracks roughly with the size of the denominator in the fractional-N synthesizer. This is the sum of Qp and Qp-1. Without use of the wrapper, this value is 25, but using the wrapper, this value is reduced to 5. Though the improvement in jitter is slight, the calculation module will always use the wrapper synthesizer, when it can, to lower output jitter.

You could launch the download module at this time, or you could just hit the "Use These" button. If not already running, clicking this button will cause the download module to launch. Whether already running or launched, this button will also copy the configuration parameters from the calculation module to the download module.

Using The Download Module

The parts of the download module are shown in Figure 16.



Figure 16. The Download Module

The purpose of the download module is to download the configuration parameters calculated by the calculation module, to the SY87729/39L device. In this way, the user may test SY87729/39L before incorporating into a prototype or design. The first step is to connect the SY87729/39L evaluation board to a PC running the download application.

Next, the configuration parameters are entered. Lastly, the configuration is downloaded and it is verified that no errors in the configuration parameters have occurred.

The first step is to launch the download application, and to connect the PC, through a printer cable, to the SY87729/39L evaluation board. This is detailed below. Before plugging the PC to the SY87729/39L evaluation board, the top right of the download application will say "No Board Found," and a yellow light will display. Once you plug the PC into a board that is powered up, the top right will look either like that in Figure 17 or in Figure 18.

[m] 739ev		
Qp	3	739 NDT locked
Qp-1	2	
P	22	
Post Div	1	739/iei
м	15	Download
N	16	Exit

Figure 17. SY87729/39L Not Locked

Figure 17 shows what often happens when you connect an SY87729/39L evaluation board that was just powered up, but has not yet accepted a download. The top right of the download application says, "739 NOT Locked,"or "739 Locked," and a red light appears. You can also get a red light if there is no suitable frequency provided to the reference inputs, REFCLK+ and REFCLK–.

(in)739er		
Gp	3	739 LDCKED
Qp-1	2	
P	22	· · · ·
PastDiv	1	739fer
м	15	Download
N	16	Exit
Configuratio	an Sent	

Figure 18. SY87729/39 Locked

The more common situation of an attached SY87729/39L evaluation board is like that in Figure 18. Here, the status at the top right says, "739 Locked" or "739 NOT Locked", and a green light appears. In this case, the correct output frequency will appear at the CLKOUT+ and CLKOUT– connectors of the SY87729/39L evaluation board.

When you get either a red light or a green light the download application indicates, in the status, whether the evaluation board has an SY87729L or an SY87739L.

Once you have connected the SY87729/39L evaluation board to the PC and launched the download application, and once you've gotten either a red light or a green light, it's time to enter the configuration parameters. You could manually compute the values of the six configuration parameters, and then enter them yourself along the left side of the download application, or you could click the "739ifier" button. This launches another copy of the calculation module. As explained above, once you've got the desired output frequency in the calculation module, you can select its "Use These" button. This will copy the configuration parameters it had calculated into the download module for you.

In fact, that's just what was done to obtain the above figures. Figure 16 shows the download application before the SY87729/39L evaluation board was attached, as per the following section. After attachment, the calculation module was set up just like in Figure 15. After selecting the "Use These" button, the download application looked just like that in Figure 17. Note that the configuration parameters computed and displayed in the calculation module match those entered in the download module.

The final step is to effect the actual download. To do this, click the "Download" button in the download application. At this point, it is VERY IMPORTANT to check the contents of the status line, which appears below the configuration parameters. This line is updated whenever the user clicks the "Download" button. If you get some message like in Figure 16, then the configuration is incorrect, and the download was not performed. This will not happen with configurations sent by the calculation module, but may occur if parameters are entered or modified manually.

Possible errors are shown in Table 2.

Error Message	Definition
QP ! = 0-31	You have entered some number greater than 31 in the "Qp" configuration edit box. This parameter may only take a number between 0 and 31 inclusive.
QPM1 ! = 0-31	You have entered some number greater than 31 in the "Qp-1" configuration edit box. This parameter may only take a number between 0 and 31 inclusive.
QP + QPM1 > 31	The sum of the values of the "Qp" and the "Qp-1" configuration edit boxes must also be some number between 0 and 31 inclusive. The download module cannot determine which of these two parameters is in error.
P ! = 17-32	You have entered some number less than 17 or greater than 32 in the "P" configuration edit box. This parameter may only take on a value between 17 and 32 inclusive.
PostDiv ! = 1-16, 18, 20, 22, 24, 26, 28, 30, 32, 36, 40, 44, 48, 52, 56, 60	The value in the "PostDiv" configuration edit box may only be one of the values listed.
MDIV != 15-18, 31-32	You have entered some number not allowed in the "M" configuration edit box. This parameter may only take on a value of 15, 16, 17, 18, 31, or 32.
NDIV != 15-18, 31-32	You have entered some number not allowed in the "N" configuration edit box. This parameter may only take on a value of 15, 16, 17, 18, 31, or 32.
MDIV, NDIV, one is 15-18, other is 31-32	The value in the "M" configuration edit box limits the choices available in the "N" configuration edit box, and vice versa. If the "M" configuration edit box contains one of 15, 16, 17, or 18, then the "N" configuration edit box must also contain one of 15, 16, 17, or 18. If the "M" configuration edit box contains one of 31 or 32, then the "N" configuration edit box must also contain one of 31 or 32.

 Table 2. Possible Error Messages

The status line will have a different message if there were no errors in the configuration. For example, starting with the download application looking like Figure 17, if you click the "Download" button, you should end up with the download application looking like Figure 18. Note that the status line says "Configuration Sent". Unless these two words appear in the status line after selecting the "Download" button, the configuration was not sent due to some error.

For those users who have two SY87729/39L evaluation boards connected to LPT1 and LPT2, you must sometimes swap which parallel port to download to. In the system menu, there is an item labeled "Swap I/O." Selecting this menu item switches between LPT1 and LPT2. The title bar changes to indicate which parallel port is currently active. A title bar like in Figure 16, that just says "739ev," indicates that LPT1 is being used for downloads. If the title bar says "739ev - LPT2," then LPT2 is being used for downloads. Please note that, if using "Direct-IO", and if it's not configured to allow I/O access to both parallel ports, selecting LPT2 will cause the program to be terminated by the operating system.

Using an External Signal Generator and Measuring Frequency Output

Now we will delve into the hardware aspects of the SY87729/39L evaluation board, and assume that you have installed and configured the applications, and are somewhat familiar with them.

This section describes how to set up a test configuration similar to that in Figure 1, where an external clock source feeds the SY87729/39L evaluation board, and a frequency counter verifies the resultant output. You will need:

- A power supply
- A frequency counter
- A signal generator
- A 50Ω termination SMA
- A SY87729/39L evaluation board
- A PC with the evaluation software installed
- A printer cable

The following steps allow the user to verify frequency of operation of the SY87729/39L evaluation board:

1. Connect Power Source: The power supply should be set to about 3.3V. Current consumption will be between 250mA and 300mA. Connect the positive power supply to the red or yellow banana jack, J1, labeled " V_{CC} " under it on the silk screen. Connect the negative power supply to the black banana jack, J2, labeled "GND" under it on the silk screen.

2. Connect Clock Source: Set your clock source to generate LVPECL level signals at the input frequency of interest. For LVPECL, the voltages are referenced to V_{CC}, so the voltage to set the signal generator to depends on the value of V_{CC}. For a V_{CC} of 3.3V, the high level of the clock signal should be between 2.135V and 2.42V. The low level

of the clock signal should be between 1.49V and 1.825V. Set the high and low levels to something like 2.3V and 1.6V. The frequency should be in the tens of Mega-Hertz. Connect this clock source to REFCLK+ and REFCLK– (J3 and J4) via SMA patch cables.

The SY87729/39L evaluation board is meant to be run with a differential clock input. Though we don't recommend it, you may feed a single-ended PECL clock on one input, and bias the other input, via a power supply, to about 2.0V. Expect a more jittery output clock in this case.

In the set up in Figure 1, an HP8133A signal source generates the clock. The clock frequency was chosen to be 25MHz. Since the 8133A only goes down to 32MHz, the frequency was set to 100MHz with a post-divide of 4. In addition, since the 8133A's edges are very fast, the clock output edges were slowed down with a pair of 2000ps transition time converters (HP15438A), one on each of the complementary outputs of the 8133A.

3. Connect Configuration Source: Attach the printer cable between the PC parallel port and the SY87729/39L evaluation board's Centronics plug, J9. Launch the download software and verify that either the message "729 Locked," "729 NOT Locked" or "739 Locked," "739 NOT Locked" appears at the upper right of the download application window.

4. Configure the SY87729/39L Evaluation Board: Launch a calculation module, and set the "Reference" edit box to the frequency of the clock source. Enter the target frequency in the "729 Output" or "739 Output" edit box and have the calculation module determine the configuration parameters. Have the download module configure the SY87729/39L evaluation board, and verify that the indicator at the upper right of the download application is green, and that it says "729 Locked" or "739 Locked."

5. Verify Output Frequency: Connect a frequency counter, capable of measuring the expected output frequency, and terminating into 50Ω , to CLKOUT+, J5, via an SMA patch cable. Connect a 50Ω termination to CLKOUT–, J6. Verify that the frequency counter indicates the expected output frequency.

Using the Supplied Reference Oscillator and Measuring Jitter

This section describes how to set up the test configuration in Figure 2, where the SY87729/39L evaluation board's internal clock source is used, and the output jitter is measured. You will need:

- A power supply
- A TIA (Time Interval Analyzer)
- Two 1-foot long SMA patch cables, length matched
- A 50 Ω termination SMA
- A SY87729/39L evaluation board
- A PC with the evaluation software installed
- A printer cable

The following steps allow the user to verify cycle-to-cycle jitter of the SY87729/39L evaluation board:

1. Connect Power Source: The power supply should be set to about 3.3V. Current consumption will be between 250mA and 300mA. Connect the positive power supply to the red or yellow banana jack, J1, labeled " V_{CC} " under it on the silk screen. Connect the negative power supply to the black banana jack, J2, labeled "GND" under it on the silk screen.

2. Connect Clock Source: Use one of the two length matched SMA patch cables to connect XTAL+ (J8) to REFCLK+ (J3). Use the other of the two length matched SMA patch cables to connect XTAL- (J7) to REFCLK- (J4).

3. Connect Configuration Source: Attach the printer cable between the PC parallel port and the SY87729/39L evaluation board's Centronics plug, J9. Launch the download software and verify that either the message "729 Locked," "729 NOT Locked" or "739 Locked," "739 NOT Locked" appears at the upper right of the download application's window.

4. Configure the SY87729/39L Evaluation Board: Launch a calculation module. Enter the target frequency in the "729 Output" or "739 Output" edit box and have the calculation module determine the configuration parameters. Have the download module configure the SY87729/39L evaluation board, and verify that the indicator at the upper right of the download application is green, and that it says "729 Locked," or "739 Locked." 5. *Verify Output Jitter*. Connect CLKOUT+ (J5) to a TIA that terminates into 50Ω . Connect a 50Ω termination to CLKOUT– (J6). Measure the cycle-to-cycle jitter.

In the set up of Figure 2, a Wavecrest DTS-2079 is used. It measures higher jitter than what is actually produced by the SY87729/39L evaluation board because of the singleended nature of the Wavecrest inputs. Alternatively, a sampling scope with histogram capability could be used, along with a delay line, where the signal input is the CLKOUT+ signal and the trigger input is the CLKOUT– signal. Also, a high-speed real-time scope may be used with Amherst M1 jitter analysis software.

Because the SY87729/39L generates clock frequencies that are other than integer ratios of the input frequency, some forms of jitter measurement cannot be taken with certain types of test equipment. This is especially true when using sampling (sometimes called equivalent time) scopes to measure jitter histograms, as these require a trigger signal separate from their input. Unless the SY87729/39L is configured to perform an integer multiply, the trigger to the scope can only be the complement clock output.

EVALUATION BOARD SCHEMATICS

Figure 19 is the schematic for the SY87729/39L evaluation board. U1 is the device being highlighted. The LVPECL input is DC coupled and terminated via R3, R4, R5 and C6. This network biases R5 at about 1.3V. Thus, the LVPECL source driving J3 and J4 sees 50 Ω (AC via C6) to about V_{CC}-2.0V. The output is AC coupled. R12 and R13 provide a DC path to ground for the CLKOUT+ and CLKOUT-LVPELC outputs, while C4 and C5 form the DC block. U3 is a crystal oscillator that provides differential LVPECL outputs directly. To use this frequency source, connect J7 to J3 and J8 to J4.

U2, a 5V tolerant buffer, interfaces the SY87729/39L evaluation board to the printer port. When not plugged in, R9 disables the outputs of U2A, allowing R6, R7, and R8 to pull down and disable U1's programming interface. When J9 pin 4 is low, U2A is enabled, U1 pin 6 is set active high, and the software on the PC can toggle PROGDI and PROGSK to effect a configuration download.

The interface always sees the state of U1's LOCKED pin. Also, one bit from the output, bit 4 (pin 5), is inverted and sent back to an input on the Centronics interface (pin 11). This is how the applications software determines whether or not an SY87729/39L evaluation board is attached to the parallel port.



Figure 19. SY87729/39L Evaluation Board Schematic

BILL OF MATERIALS

Item	Description	Qty.
C1	22µF, 16V "C" Size, Tantalum Electrolytic Capacitor	1
C2, C3, C4, C5	100nF, 10V X7R Size 0603 Ceramic Capacitor	4
C6, C7, C8 C9, C10, C11 C12, C13, C14	0.1µF, 10V Size 0805, Ceramic Bypass Capacitor	9
J1	Banana Jack Binding Post, Yellow or Red	1
J2	Banana Jack Binding Post, Black	1
J3–J8	SMA Edge Launch Connector	6
J9	Centronics 36-Pin Right Angle Connector	1
L1	Ferrite Bead, Size 0805	1
R1, R2	2.00kΩ, 1% Size 0603, 1/10W Resistor	2
R3, R4, R5	51.1Ω, 1% Size 0805, 1/10W Resistor	3
R6, R7, R8	10kΩ, 1% Size 0805, 1/10W Resistor	3
R9, R10	2.21kΩ, 1% Size 0805, 1/10W Resistor	2
R11	475Ω, 1% Size 0805, 1/10W Resistor	1
R12, R13	121Ω, 1% Size 0603, 1/10W Resistor	2
R14, R15	In-Line Place to Install Optional Back-Termination Resistors	2
U1	Micrel's SY87729/39L Frequency Synthesizer	1
U2	5V Tolerant Dual 4-Bit Buffer	1
U3	27.000MHz Oscillator with Differential, LVPECL Outputs, DIP-14	1

ORDERING INFORMATION

Evaluation Board Part#	IC Package	Operating Range
SY87729L–EVAL	EPAD-TQFP-32	–40°C to +85°C
SY87739L–EVAL	EPAD-TQFP-32	–40°C to +85°C

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